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ELECTRONIC DESIGN

NOVEMBER 1, 1993

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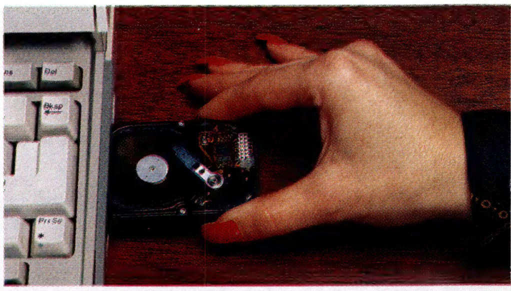

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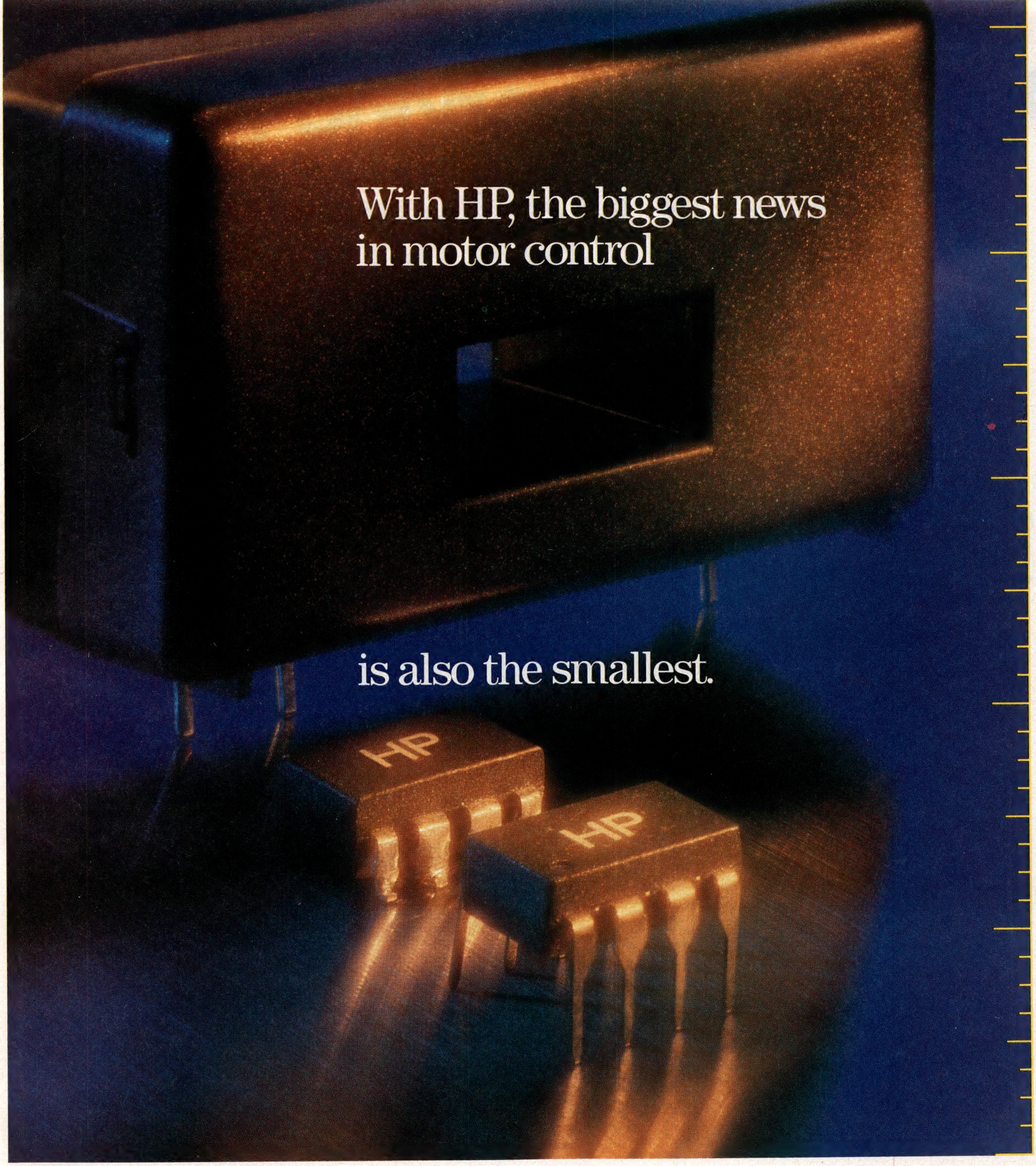

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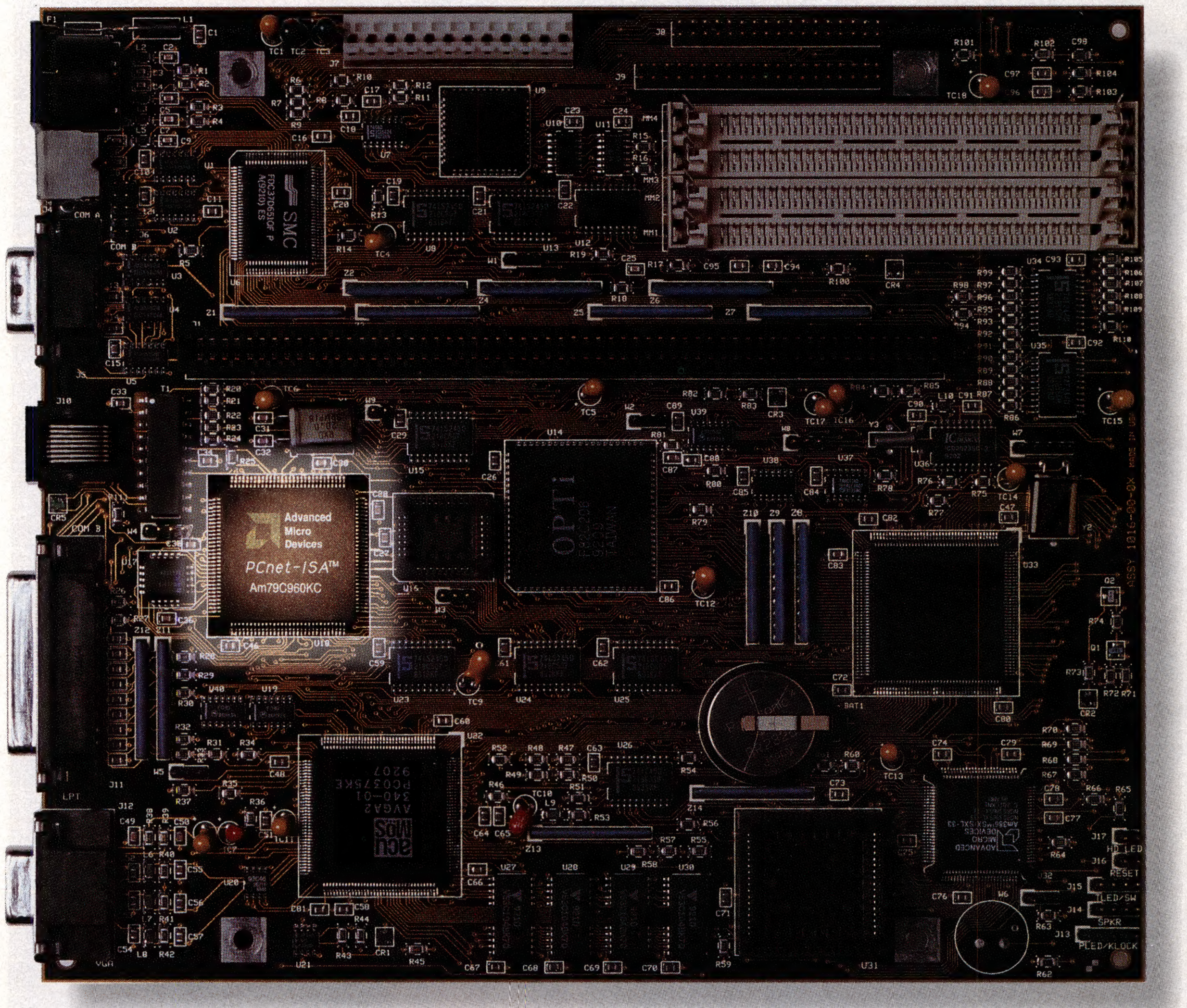

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NOVEMBER 1, 1993 VOL. 41, NO. 22

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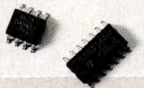

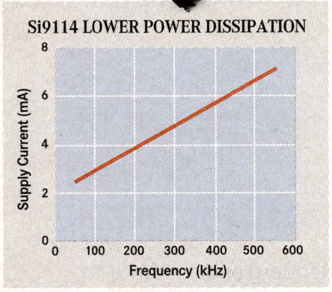

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ONE VOTE FOR THE NAFTA

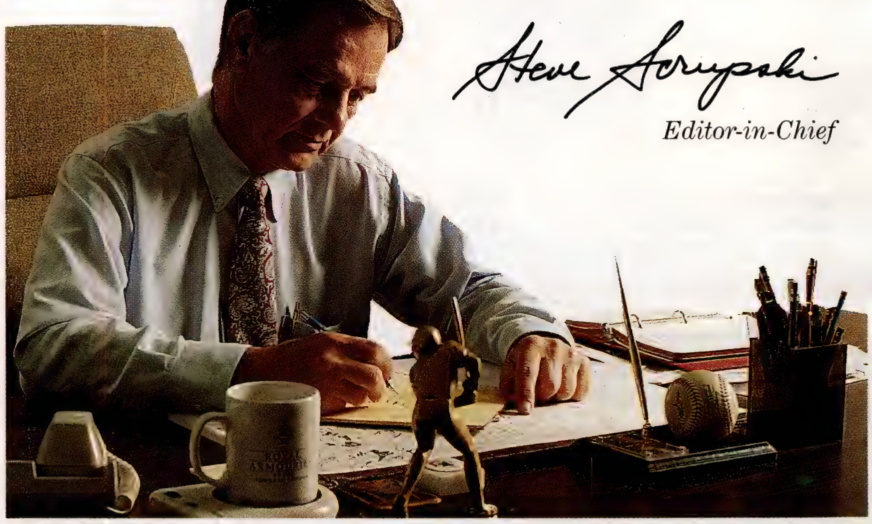
What's your take on the North American Free Trade Agreement? Some cogent arguments are being made on each side: potential job losses and potential environmental damage versus expanded sales and rising employment. Others say the more free trade throughout the world, the better off we all will be.

It's a tough call, but overall, the bottom line is that the NAFTA will be good for the U.S. electronics industry. There are other agreements that would be even better, such as freer trade with many other countries, but it seems inescapable that U.S. electronics manufacturers, engineers, and manufacturing workers will benefit from the NAFTA. For example, take what the American Electronics Association, which has endorsed the NAFTA (as have other organizations such as the Computer Systems Policy Project, made up of CEOs of the 13 largest computer makers), says:

"Our members (the AEA consists of 3000 member companies, more than 80% of which have fewer than 200 employees) will derive their principal business advantage from the NAFTA's stimulus to the growth of the Mexican economy. Mexico is already our third largest trading partner, and it purchases more U.S. goods per capita than does Europe....Currently, most electronics products enter the U.S. from Mexico duty-free; the NAFTA will achieve equal status for U.S. products entering Mexico, which now face high duties. This will provide a strong incentive to retain jobs in the U.S."

However, many people have misgivings about the agreement, fearing a loss of manufacturing jobs in the U.S. No one should dismiss as unfounded such a concern over manufacturing jobs going South. In fact, as some supporters have admitted, the chances are good that this will happen in those industries where manufacturing labor is relatively unskilled. But it's difficult to believe that, with all of today's emphasis on quality and ISO 9000 programs, U.S. electronics manufacturers who invested in quality programs and worker training as well as set up quality improvement teams among their workers will opt to go South and start all over, simply because one element of their production costs—manufacturing labor—is lower elsewhere. They already have had ample opportunities to make such a move.

As far as electronics is concerned, though, there are bigger problems than those found on the North American continent. We'd like to see as much effort put into toughening up the trade negotiations with our other trading partners around the world as is now going into selling the NAFTA to Congress and the American public. In the meantime, we will tilt in favor of the NAFTA.



Steve Scrupski

Editor-in-Chief

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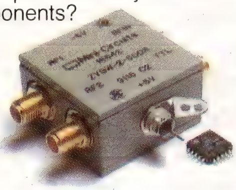

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Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	—	20	—	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
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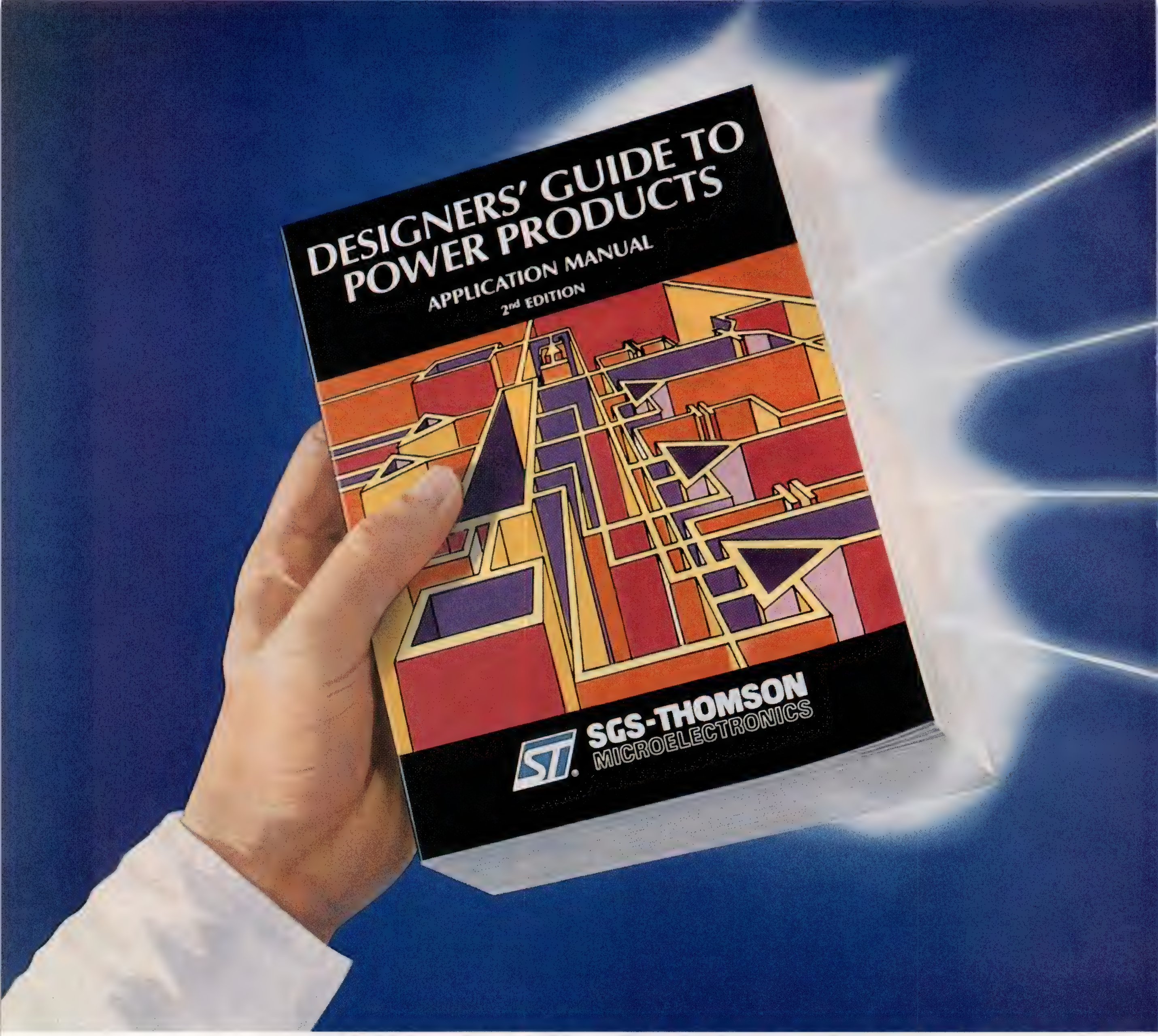

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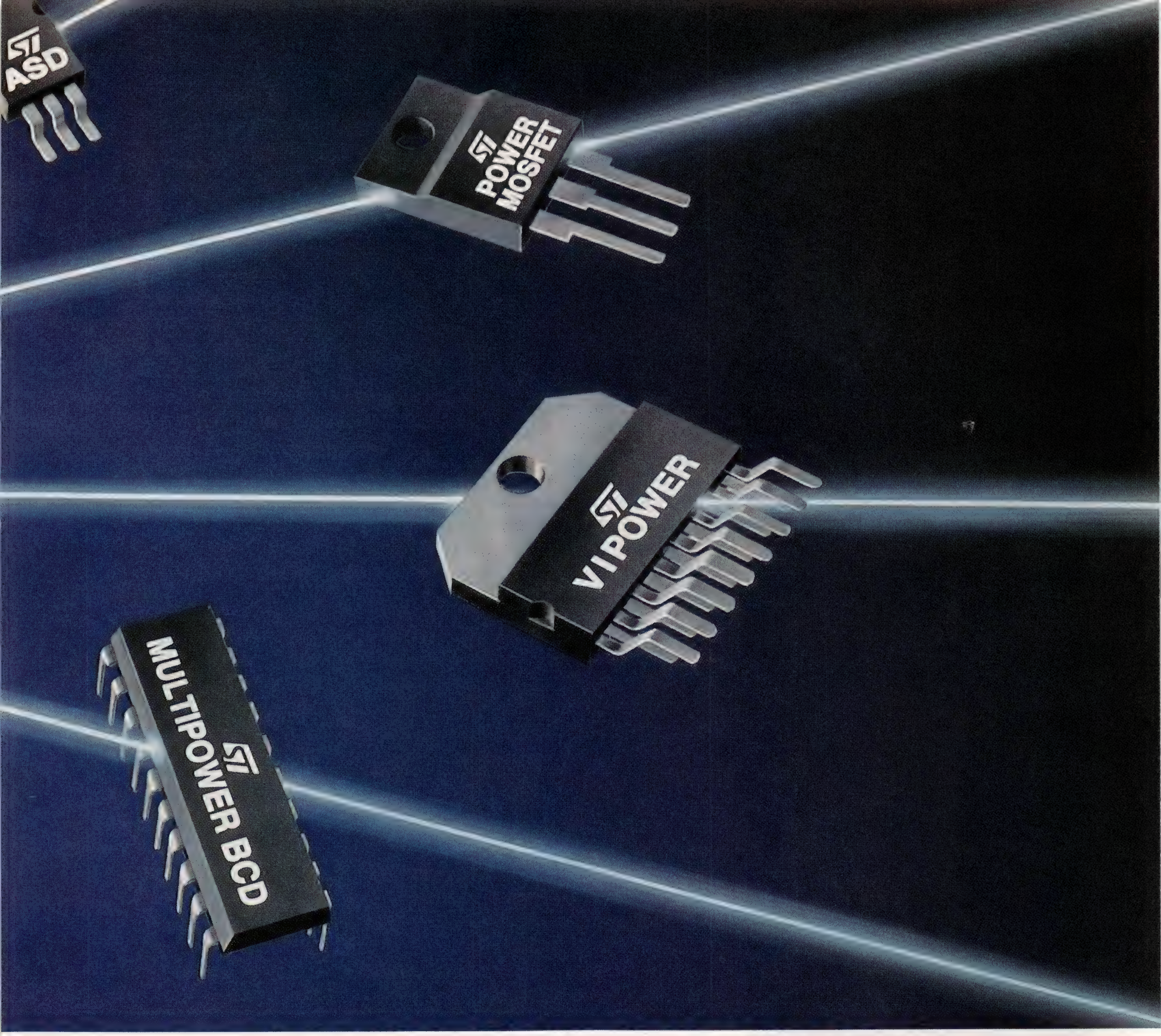

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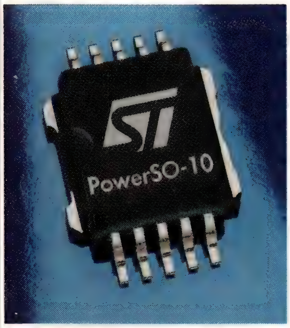

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Opening Windows On Embedded Design

When developing embedded systems, designers typically work with tools from several sources. Some development environments include most or all of the tools needed, while other designers prefer to write their own kernels and use third-party libraries, compilers, linkers, and debuggers. That variety in embedded development also extends to platforms: Electronic Design's reader surveys show that most engineers use both a PC and a Unix workstation. Which machine a designer fires up depends on the tools used and the size of the project—larger projects usually entail networked workstations. Currently, twice as many PCs as Unix workstation seats are purchased for application development, according to a recent International Data Corp. (IDC) survey. On either platform, getting the embedded development tools to work together isn't a simple task; nor is the source of trouble easy to trace when several products and companies are involved.

However, some relief may be at hand. The Windows user interface for PCs is making inroads for designing at a much slower pace than in commercial settings, yet Unix tools for embedded design, along with Windows, are being ported to the PC. Windows' dynamic-link-library (DLL) features help connect data among programs, though memory allocation and timing demands in real time must be deftly managed. Developers can set breakpoints in applications, view the C code in a window, and then look at the underlying assembly code. A drawback is a development team working on the same code needs a networked version to track changes. Unix workstations' built-in sockets clearly hold the advantage in the ease of linking a project's developers.


SHERRIE VAN TYLE
SOFTWARE

"Developers either like Windows or they hate it. But it's here," says Jack Ganssle president of Softaid, a Columbia, Md., company that makes emulators and a source-level debugger for Windows. Ganssle says his company's survey of embedded developers revealed that 80% want Windows, a big change from a survey conducted a few years ago when most turned it thumbs down.

Tom Barrett of A.T. Barrett & Associates based in Houston, Texas, whose company's RTXC kernel supports Motorola, Intel, and Siemens processors, among others, says there's interest in integrating the company's own tools with others: "We want to deliver a set of tools that enable a developer to create an application and test it without having to integrate compilers and source-level and system-level debuggers."

Pleasing to some, Windows' pull-down menus, as well as its pointing and clicking mode of operation, irritate others. Developers who cut their teeth on DOS may still prefer to rattle off commands from the keyboard onto the command line. To ease the conversion, tool makers often incorporate a choice of entering commands, either DOS-style or the point-and-click mode of a Windows interface.

Mike Mahar, project manager at Microtec Research, Santa Clara, Calif., whose Windows version of the XRAY MasterWorks development environment is slated for release early next year, declares "It's not shipping unless developers will be able to do everything they want to do." For instance, built into the user interface is a window for entering commands DOS-style. In addition, built around the Windows dialog box, a command notebook records user requirements and lists commands that are complex and difficult for developers to remember, such as test-coverage commands.

The headaches incurred when networking is added to a group of PCs running development tools should be eased with Windows NT's networking features. Among other companies porting to Windows, Wind River Systems, Alameda, Calif., will release a Windows version of its VxWorks development software in January.

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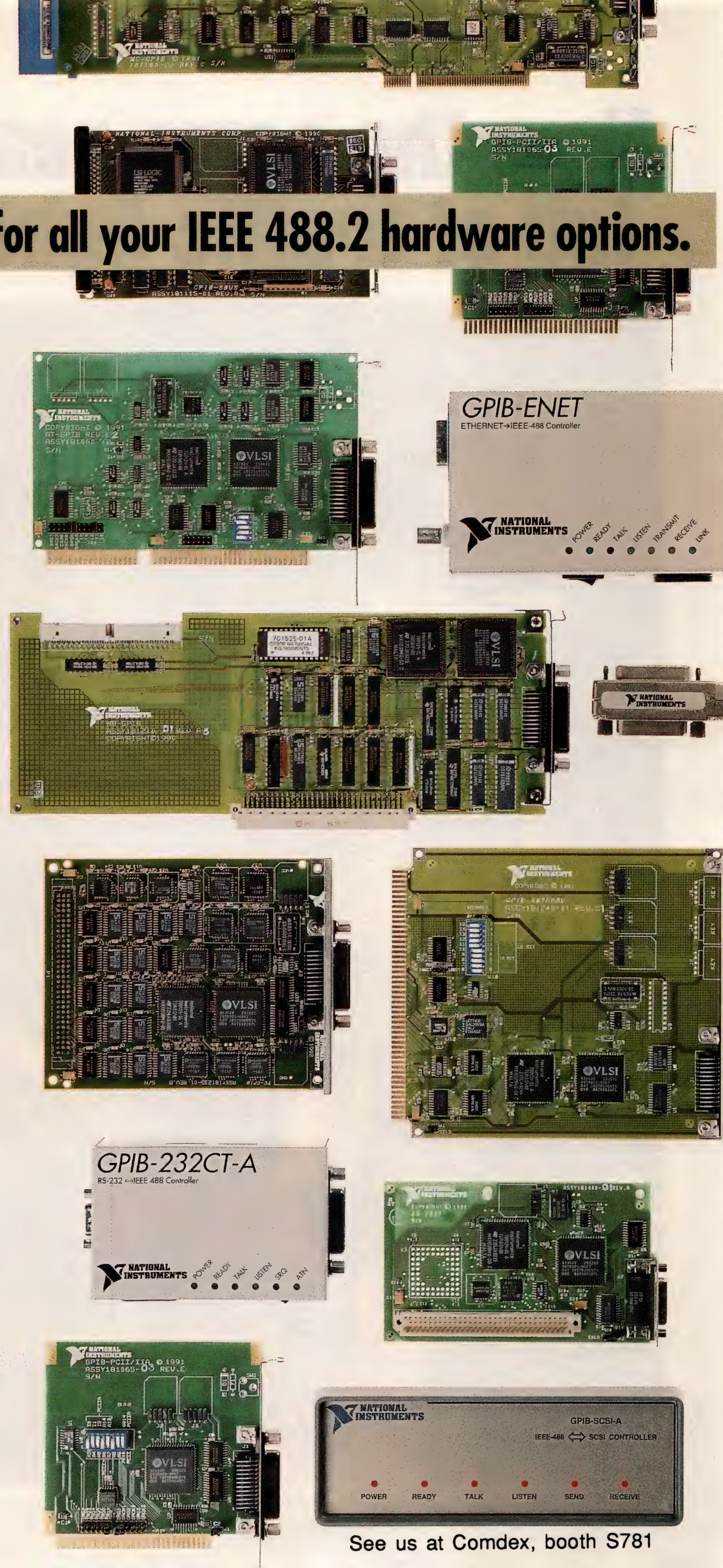

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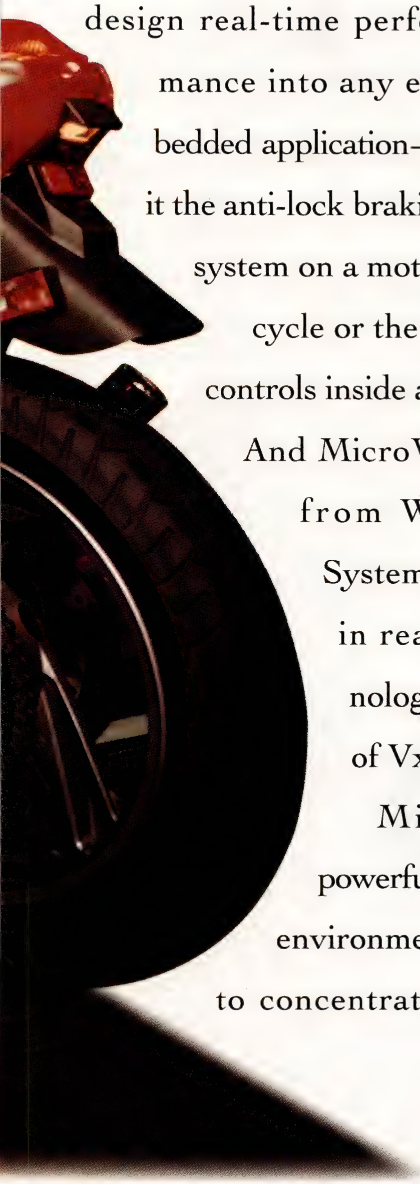

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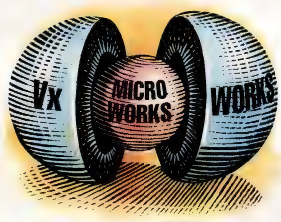

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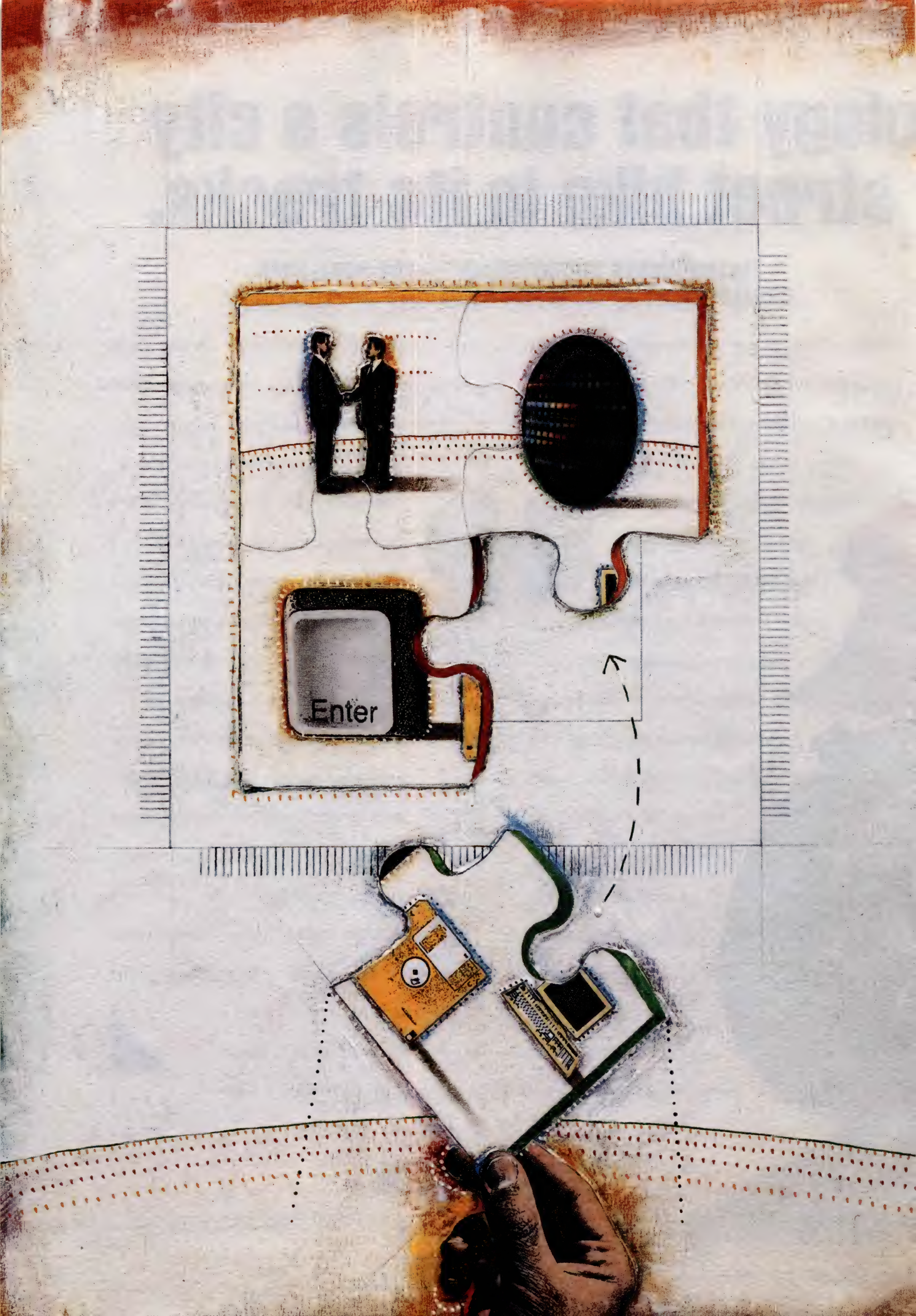
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CIRCLE 124

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After six months of being exposed to one commercial, awareness of colon cancer among adults 40 and over rose from 11% to 29%.

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TECHNOLOGY NEWSLETTER

ALLIANCE FOCUSES ON MCM PROCESSING

Cost-efficient, multichip-module processing techniques are the goal of a research affiliation between The Dow Chemical Co., Midland, Mich., and the Electronic Technologies Division of MCNC, Research Triangle Park, N.C. The research project will center on developing less costly techniques for applying Dow's photoimageable benzocyclobutene (BCB) dielectric coatings. The photoimageable-polymer dielectrics are expected to facilitate the elimination of costly patterning methods, such as plasma etching, as well as the required sacrificial-masking layers. The developmental photoimageable BCB derivatives are processed by a thermal cure that uses no catalysts. For more information, contact Dow Chemical at (800) 441-4369. *DM*

INTUITIVE DATA SPEEDS IC-LAYOUT PROCESS

A recently unveiled symbolic layout editor can accelerate IC layout by up to ten times over conventional polygon design methods. The editor uses object-oriented techniques to represent layout data in an intuitive fashion that's more familiar to IC designers than the loose, stick representations traditionally employed by symbolic design tools. The Rose editor can speed up layouts because it uses graphics that closely resemble the actual physical layout. Rose is based on research and development done by Rockwell International Corp., Newport Beach, Calif., and is available from Compass Design Automation Inc., San Jose, Calif. It supports 45° geometries, which results in layout-density improvements of up to 10% over symbolic tools that handle only orthogonal geometries. In addition, Rose can automatically retarget IC layout at the chip level. For more information, call Compass Design Automation at (408) 433-4880. *LM*

TINY SWITCHER POWERS PCMCIA TYPE I CARD

By operating at a switching frequency of 500 kHz, a 12-V-output dc-dc converter in a 20-lead TSSOP case meets the 3.3-mm maximum-height specification for Type I PCMCIA cards. The converter chip, complete with a 0.5-A 300-mV power switch, is the first such device to meet the PCMCIA specification. It was designed by Linear Technology Corp., Milpitas, Calif. (the LT1106). Running at such a high frequency allows the chip, as well as the required capacitors and an inductor from Coiltronics, Boca Raton, Fla., to meet the thin PCMCIA height specification. The converter and related components are used on Intel's recently introduced flash memory cards *(see "Portable system users can take 40 Mbytes on the road," p. 107)*. If the PC's PCMCIA socket doesn't provide the card with power, the converter will. It operates in a burst mode switching at 85% efficiency. Contact Bob Scott at Linear Technology at (408) 432-1900. *FG*

ANTENNA ALGORITHMS CALCULATE SYSTEM EMI

Engineers can accurately calculate the EMI radiating from multichip modules and pc boards thanks to an analysis tool that uses loop-antenna principles with physical-layout information. The analysis software, called ContecRadia, was developed by Contec Microelectronics USA, San Jose, Calif. First, systems are modeled as analog behavioral- or transistor-level circuits, and layout conductor traces are modeled as multiple-coupled lossy transmission lines. ContecRadia automatically extracts the electrical models from layout files using the company's electromagnetic field solver. Then, the company's circuit simulator determines the time-domain current and voltage distributions in the conductor traces. Using the current distribution on the conductive traces, the radiated electric field intensities are calculated based on loop-antenna principles. ContecRadia determines the electrical effects, reflection, and crosstalk coming from transmission lines in high-speed digital, analog, and mixed-signal systems. And because of advanced algorithms, ContecRadia simulates nonlinear mixed-signal circuits faster than Spice. Call (408) 434-6767 for more information. *LM*

LICENSE MERGES FLASH WITH MICROCONTROLLERS

A combination development and patent licensing agreement between Zilog Inc., Campbell, Calif., and Catalyst Semiconductor Inc., Santa Clara, Calif., gives Zilog nonvolatile flash-memory technology and Catalyst one-time programmable EPROM capability. Consequently, Zilog will be able to develop Z8-based microcontrollers with embedded flash and Catalyst can now expand into non-memory areas with Z8-based controllers. The two also plan to jointly develop future Z8-based products that employ flash technology. First samples of the first flash-based Z8 microcontrollers are expected in the

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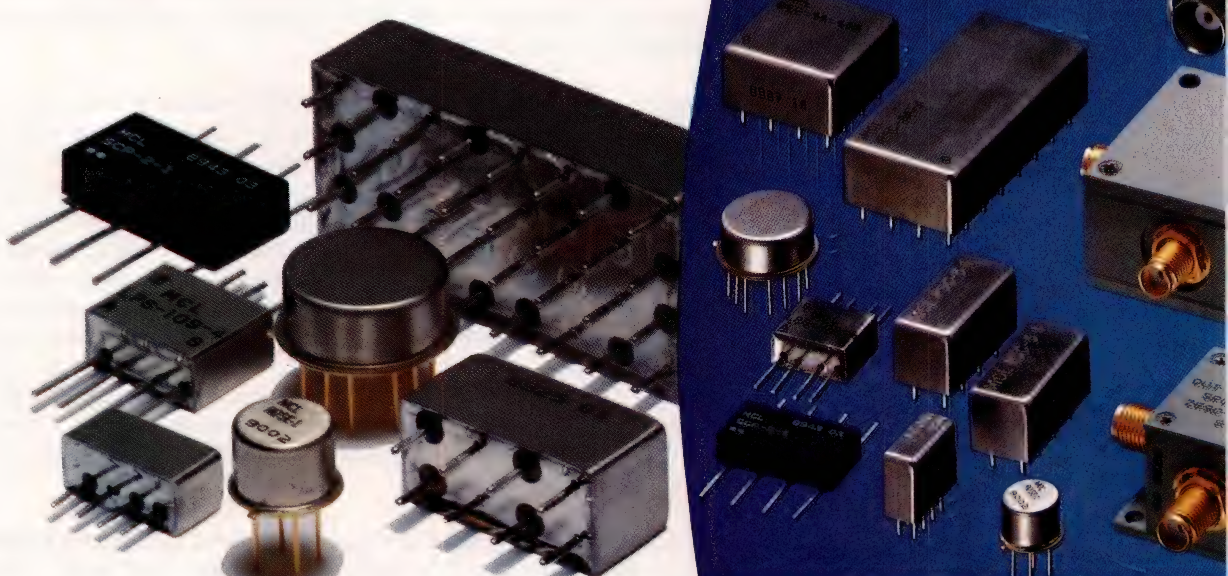

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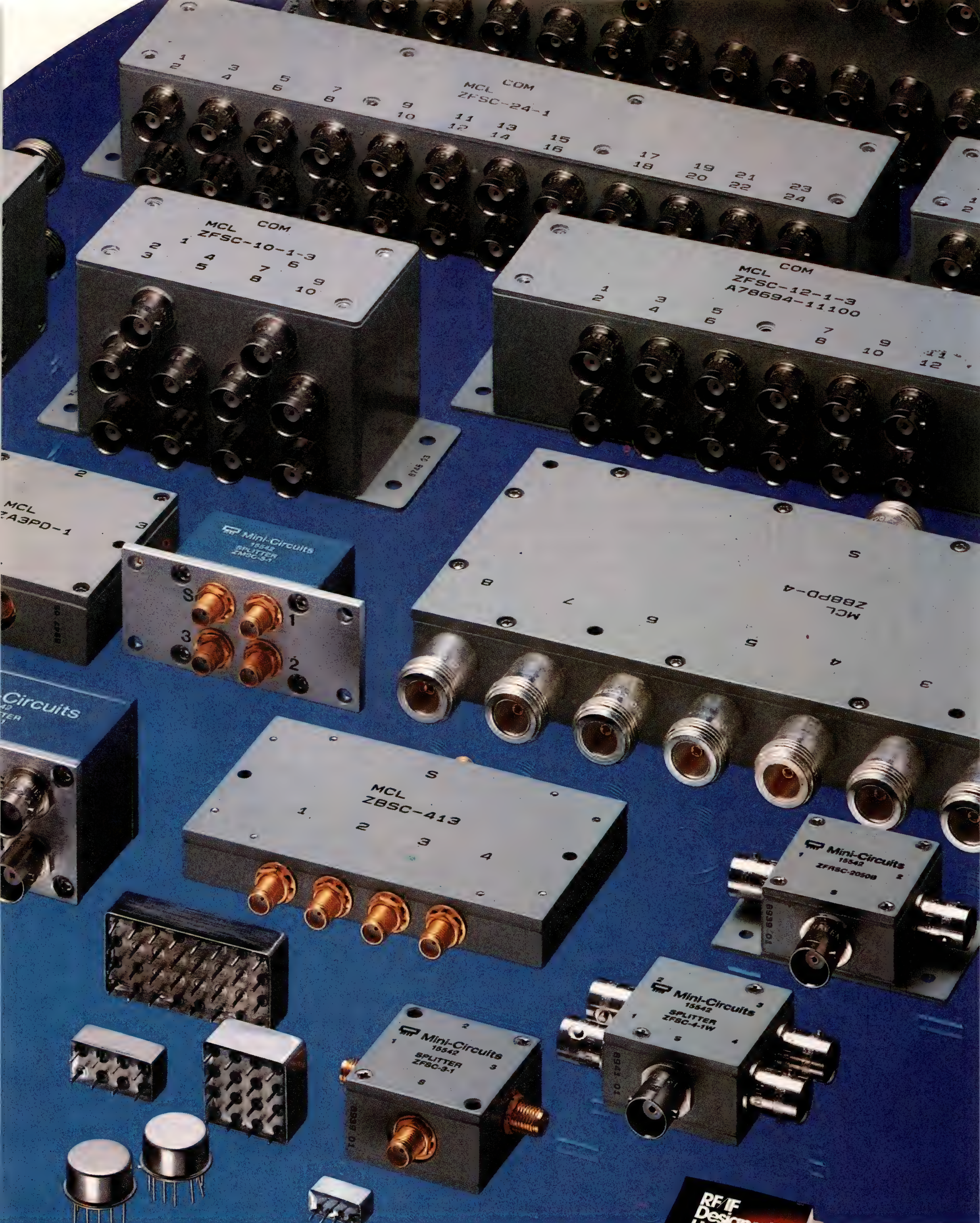

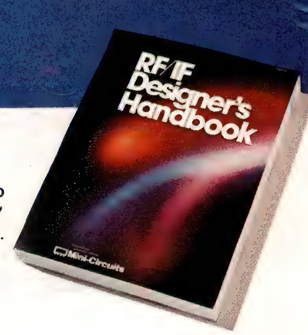

For detailed specs on all Mini-Circuits products refer to
• THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCT DIRECTORY
• EEM • MINI-CIRCUITS' 740-pg HANDBOOK.

second quarter of 1994. Merging flash and controller technologies allows the companies to create single-chip reprogrammable controllers that don't require the expensive windowed packages used by UV EPROM-based controllers. *DB*

Liquid System Cools Pentium-Based Notebooks

As concerns mount regarding the cooling of today's fastest, hotter-running microprocessors, a scheme for fluid cooling of notebook computers may be one way around the problem. The Oasis cooling technology, developed by Aavid Engineering Inc., Laconia, N.H., is targeted at Pentium- and Alpha-based portable PCs as well as desktop units. The system precisely controls device temperatures at a level that assures reliable operation at the fastest possible speeds. Composed entirely of flexible materials, the cooling scheme requires as little as 0.25 in. of space atop the microprocessor, enabling it to be sandwiched between boards if necessary. Leak-proof materials that were developed for medical applications are used, as is an inert, non-toxic, non-flammable, and non-ozone-depleting liquid coolant. For information, call Gary Kuzmin at (603) 528-3400. *DM*

Consortium Pushes For Standard Analog HDL

To accelerate the development and standardization of the IEEE's VHDL-A analog hardware description language (HDL), a group of EDA vendors and users established the Analog VHDL International (AVI) consortium. A standard analog HDL will ease behavioral modeling, and will protect modeling investments by ensuring that models are portable across simulators conforming to the new standard. AVI will support the VHDL-A standard with such activities as creating validation suites in parallel with the IEEE's Language Reference Manual development effort. These suites will let users verify compliance to the standard as soon as the reference manual is completed later next year. Initial consortium members include Anacad EES, Analogy, BNR/Northern Telecom, Cadence Design Systems, Compass Design Automation, Hewlett-Packard, Mentor Graphics, Meta-Software, MicroSim, SGS-Thomson, and Viewlogic Systems. AVI is currently seeking additional members, including universities. Call Meta-Software's Shawn Hailey at (408) 369-5412 for membership information. *LM*

Backplane Assists In Analog Optimization

An optimization backplane is among the innovations that enable the Resolve analog-optimization software to overcome the various limitations of previous tools. No optimization algorithm alone can solve the many problems involved in analog IC, board, and system design. However, the Resolve software designed by Cadence Design Systems Inc., San Jose, Calif., creates an expandable environment with an optimization backplane. The backplane is actually a procedural interface that lets users integrate their own algorithms into Resolve without code changes from Cadence. Initially, Resolve comes with a modified-least-squares general-purpose algorithm, but development work on other algorithms is already underway. Another large obstacle in analog-optimization technology has been performance in the time domain. Resolve addresses performance problems by automatically distributing its operation across multiple CPUs on a network. In addition, Cadence combined the optimizer with its hardware-description language to optimize large analog systems. The Resolve optimization software is an option to Cadence's Analog Workbench and Analog Artist design systems. For more information call the company at (408) 943-1234. *LM*

Improved Board Drilling Under Study

Better CAD/CAM software for the design and drilling of printed wiring boards is the goal of a government-industry partnership sponsored by the U.S. Department of Energy. Under a one-year, cost-shared Cooperative Research Agreement, Los Alamos National Laboratory and Infinite Graphics of Minneapolis will try to cut board drilling times by minimizing the drill head's backtracking as it completes a complex drilling pattern. Infinite Graphics will deal with the analysis, enhancement, and design of the wiring boards, while Los Alamos will contribute in the area known as Monte Carlo codes, which are used to track random events. Also useful will be the Lab's expertise in the generation and analysis of unstructured grids used in modeling hydrodynamics. In some ways, these grids resemble the thousands of holes laid out on wiring boards. The agreement is the first under the DOE's Small Business Initiative, which gives small businesses access to the skills of department scientists through direct services, partnerships, technical assistance, and use of facilities. *JN*

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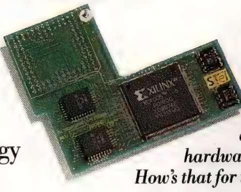

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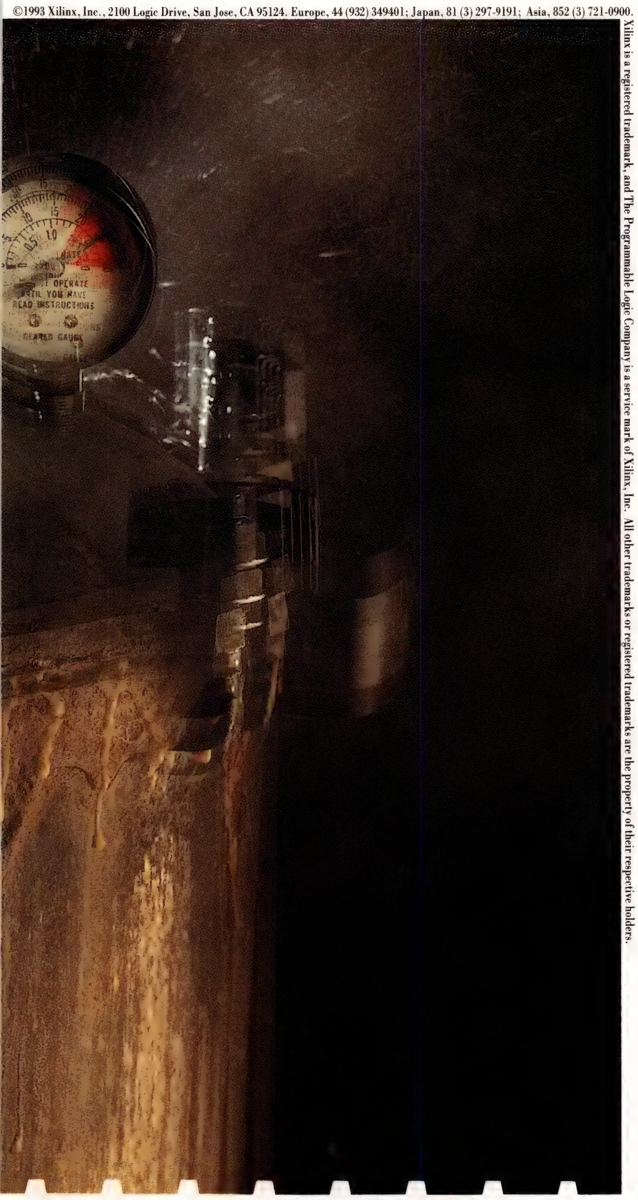

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Chart I	Actel	Actel	Xilinx	Altera
Device	A1240A	A1240A-2	XC4005A-5	EPM7256-20
Capacity [1]	15.3	15.3	15.4	14.7
Performance [2]	36.3 MHz	48.4 MHz	35.0 MHz	45.3 MHz
Price [3]	$68.80	$96.30	$138.70	$214.25

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Chart II	Actel	AMD
Device	A1225A	22V10Q-25
# Devices	1	12
Total Icc Power [4]	10 mA	660 mA
Total Price [5]	$42.50	$ 77.16

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1. Average number of PREP instances, approximately 4000 gates or 20 PALCE22V10s. 2. PREP Derived Data-average internal operating frequency, in MHz. 3. 100 piece PQFP price quoted by authorized distributor, August/September 1993. 4. Typical Icc per device multiplied by number of devices. 5. Based on 100 piece PLCC price quoted by authorized distributor, August/September 1993. ACT, PLICE, Designer, and the Actel logo are trademarks or registered trademarks of Actel Corporation. PREP is a trademark of the Programmable Electronics Performance Corporation. All other brand or product names are property of their respective holders.

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MICROMACHINING TECHNOLOGY STRIVES TO CREATE ELECTRO-FLUIDIC CONTROLLERS ON MCMS

Fluidic analogs of integrated circuits are now possible thanks to a recent development that combines a thermopneumatic actuator with sensors and other electronic components on a silicon chip. Called a Fluistor (fluidic transistor) by its developer, Redwood Microsystems Inc., Menlo Park, Calif., the microactuator is machined by photolithographic processes to respond mechanically to an electrical input in ways similar to a transistor's electrical behavior for proportional or on-off control of gas or liquid flow.

The device has already found its way into a solid-state pressure regulator and a valve-sensor manifold. But perhaps the most attractive aspect of the technology, now under development, is its ability to create complex electro-fluidic multichip modules (E/F MCMs) for precise control of gases and liquids in process control, analytical instrumentation, and medical instrumentation.

For example, Fluistor valves can be combined with pressure sensors, a microcontroller, and glue logic on a common substrate to form custom manifolds and multiplexers *(see the figure)*. These could be used in portable instruments to replace larger, more expensive electromechanical systems. Pocket-calculator-sized E/F MCM manifolds with hundreds of on-off valves can be designed to deliver pneumatic on-off signals that control valves in semiconductor processing operations.

In a Fluistor valve, the key component is a flexible membrane formed by micromachining a precisely controlled recess in a silicon substrate. A Pyrex wafer with a built-in heating (thin-film resistor) element covers the liquid-filled recess to create a hermetically sealed chamber.

Passing current through the resistor heats the liquid, which in turn expands to flex the silicon diaphragm outward toward a second Pyrex wafer bonded to the underside. This wafer contains channels and orifices designed to direct the flow of the controlled liquid.

Typical dimensions of a standard Fluistor chip are about 5.5-by-6.5-by-2 mm, with a fluid-chamber capacity of 4 μl. The basic valve design can be modified to optimize various performance capabilities. For example, a standard Fluistor can handle a gaseous flow rate of less than 1 μl/min. at a pressure of 20 psi, or up to 16 l/min. at 80 psi. Liquids have been controlled at flow rates of over 300 ml/min. at a pressure of 1 atm.

However, a larger membrane and orifice allows for higher flow rates; thicker walls on the liquid-filled chamber permit higher pressures; and suspending the heater in the control liquid could produce faster response times. Furthermore, the performance of the liquid-filled cavity can also be tailored to suit specific applications by adjusting the boiling point of the liquid, the quantity of molecules, and other properties.

As the technology advances, Redwood Microsystems expects Fluistors to be able to handle gaseous flow rates of up to 30 l/min. at 80 psi, and provide analog control of fluids at up to 6000 psi. Controlling water flow rates of over 60 ml/min. at a pressure of 1 atm will also be possible.

The company says the next challenge will be to provide Fluistor chips in a monolithic construction, with multiple sensors or valves manufactured simultaneously on a common substrate. Consequently, today's instruments—the equivalent of yesterday's mainframe computers—will be replaced by the instrumentation equivalents of workstations, laptop computers, and field-portable equipment.

For more information, call Ben Dehan at (415) 617-1200.

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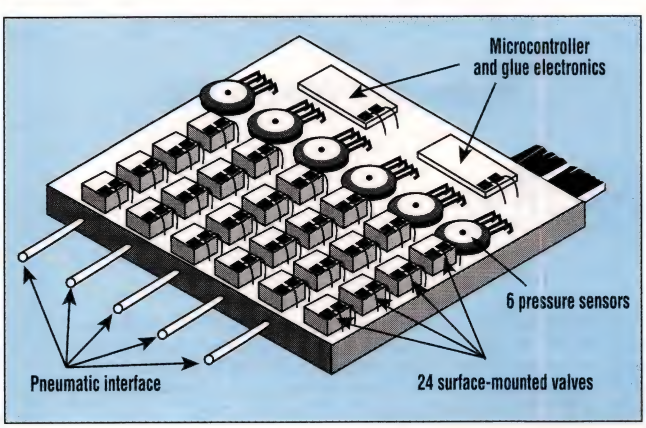

ARCHITECTURAL ENHANCEMENTS SPEED UP MICROSPARC CPU

The leapfrog game of CPU performance gains changes alternately between radical new architectures and feature-set refinements. When the Sparc RISC CPUs were introduced, it was a radical change to move from CISC CPUs to the RISC world. However, as the generations of CPUs move forward, refinements in architecture and increased on-chip resources provide the necessary performance kicks for existing architectures to keep pace with performance demands.

A case in point is the recent unveiling of the microSPARC II processor, developed by Sun Microsystems Computer Corp., Mountain View, Calif. By refining the microSPARC I's architecture, quadrupling the size of the on-chip cache, and upping the clock to 70 MHz, designers at Sun almost doubled the throughput of the microSPARC II over the original 50-MHz microSPARC I *(see the figure)*.

The microSPARC II, which the company has started to sample, contains over 2.3 million transistors that are fabricated in a 0.5-μm triple-level-metal process. It also incorporates power-management modes capable of trimming the active power by 90% when the CPU or cache idles. It's designed to oper-

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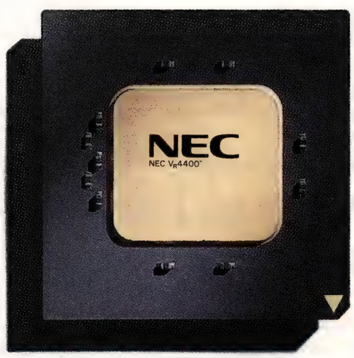

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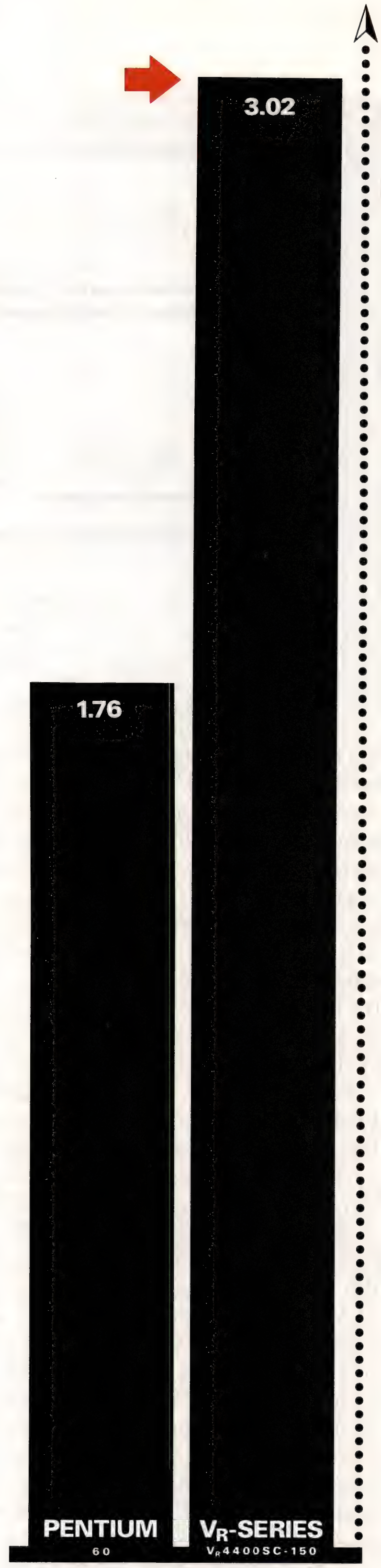
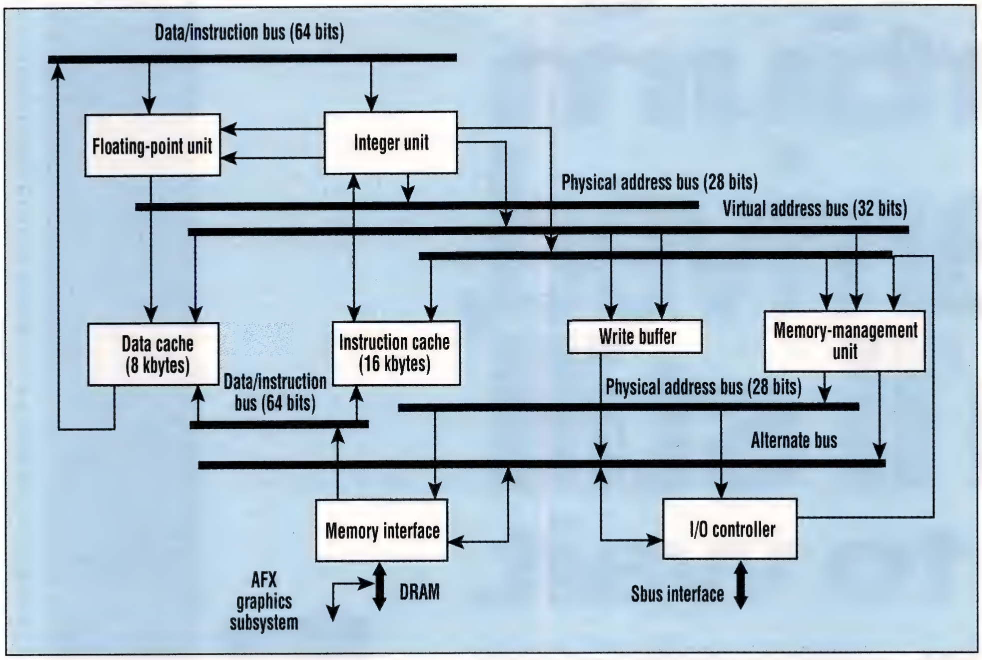
For applications and technical information, please call NEC Electronics Inc. at 1-800-366-9782. Or fax us at 1-800-729-9288 and ask for Info Pack #168.



BYTE BENCHMARK
PERFORMANCE RELATIVE TO 486-66

NEC



ate from a 3.3-V supply and tie in with either 3.3- or 5-V memory subsystems. The lower supply voltage together with the power-management feature trims the operating power to about 5 W in the active mode and to about 0.5 W in the idle mode—low enough to satisfy many portable system requirements.

Fabricated for Sun by Fujitsu Microelectronics Inc., San Jose, Calif., the microSPARC II packs 16 kbytes of instruction cache and 8 kbytes of data cache, each four times the size of the caches on the microSPARC I. Although the integer processor with its five-stage pipeline is basically the same, the CPU designers added branch folding with delayed instruction execution and static branch prediction to minimize pipeline stalls.

The microSPARC I's two-word write buffer was expanded to four double words in the microSPARC II. The larger buffer permits the CPU to immediately start the next operation, eliminating delays when several writes are performed back-to-back. Also, four instructions are fetched at a time rather than one, thus improving overall cycle efficiency. An expanded 64-entry memory-management unit (versus 32 entries on the older chip) allows the CPU to manage 256 contexts, which enhances the CPU's ability to support multitasking. The CPU also features an expanded address range of 256 Mbytes—double that of the previous microSPARC.

To accomplish more in each cycle, the register file was expanded to 136 registers so that eight register windows. Furthermore, a third read port was added to the register file so that the CPU can perform three read and one write operation every cycle. Floating-point operations were also improved by giving the floating-point coprocessor its own multiplier. The multiplier can operate in parallel with other functions, reducing the cycle time for most of the floating-point operations (in the microSPARC I, the floating-point unit shared the integer unit's multiplier). As a result, the microSPARC II can deliver throughputs of 51 SPECint92 and 43 SPECfp92 when internally running at 70 MHz.

In addition, to make systems easier to design, an on-chip phase-locked loop/clock multiplier lets designers use a 35-MHz system clock to generate the 70-MHz internal clock. The timing logic also provides an output clock for the Sbus. That clock can be set at 1/3, 1/4, or 1/5 of the internal clock. Consequently, when higher-speed versions of the CPU become available, just the division ratio need be changed when the CPUs are upgraded. Commercial release of the 321-pin microSPARC II is expected in early 1994 at a price well under $500.

The microSPARC II will be sold through a newly established business unit known as the Sparc Technology Business (STB). STB will sell existing as well as future Sparc processors and related support chips created by Sparc licensees. For more information, contact Derek Meyer at STB at (415) 336-0710.

DAVE BURSKY

ENHANCED POWERPC CPU TRIMS POWER FOR PORTABLE PCS

A strong emphasis on improving power management and efficiency exemplifies the recently released second member of the PowerPC CPU family. The MPC603 (PowerPC 603) RISC processor, fabricated in a 0.5-µm triple-level-metal CMOS process, is targeted at portable computer systems and entry-level desktop computers.

The device, jointly designed by IBM Corp. and Motorola Inc., both in Austin, Texas, had its total cache cut in half. As a result, the new processor now integrates 16 kbytes instead of the 32 kbytes that resides on its predecessor, the PowerPC 601 CPU. Furthermore, the designers decided to split that cache into 8 kbytes each for data and instructions, rather than employ the unified cache present in the PowerPC 601.

By splitting the cache, banks can be powered down when not being accessed, thus lessening the power drain. The change from unified to split caches and the reduced cache size helps to minimize the silicon-chip's area. But it also trims back performance a bit: The PowerPC 601 accesses eight instructions in one cycle, while the PowerPC 603 accesses only two instructions in

one cycle.

However, the use of split caches allow both instructions and data to be simultaneously accessed, thus compensating for the fewer instructions accessed in one cycle. Furthermore, the external bus can be set for either 32-bit-wide or 64-bit-wide operation. Support was also included for one level of address pipelining as well as out-of-order bus transactions.

The 240-pin CPU implements the 32-bit portion of the PowerPC architecture in a silicon area just 85 mm^2—about two-thirds the size of the PowerPC 601. The PowerPC 603 includes four software-controllable power-saving modes. Three of the modes—nap, doze, and sleep—are static and progressively reduce the power to just a few milliwatts. When clocked at 80 MHz, the chip will consume about 3 W and deliver a throughput of 75 SPECint92 and 85 SPECfp92. At a frequency 66 MHz, the power falls to 2.5 W and the throughput drops by about 20%.

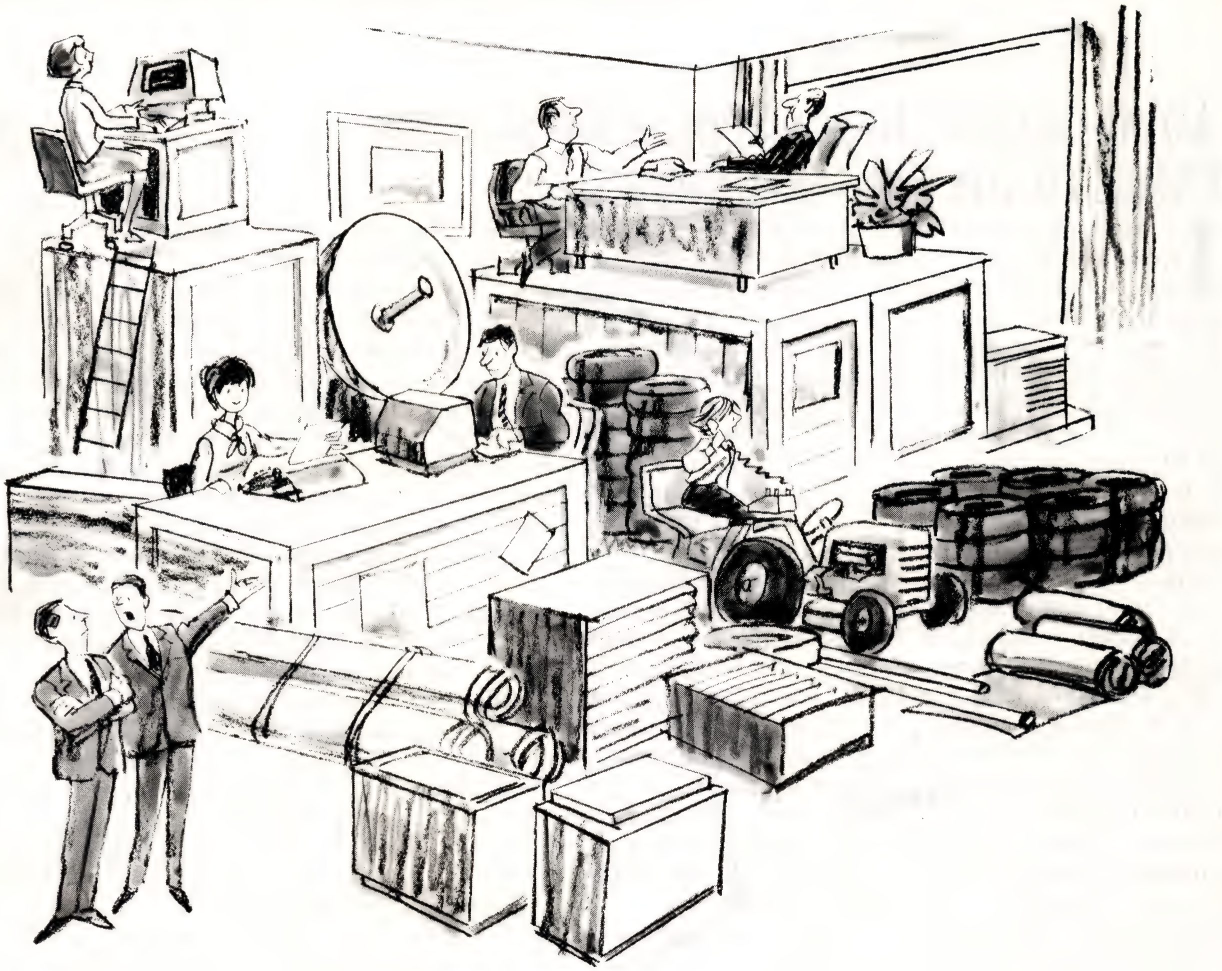
To better manage the power from the system, CPU clocking is based on an internal programmable phase-locked loop that can run at integer multiples of the bus clock. The clock ratio can be changed by first putting the chip into its sleep mode, changing the pin settings, and then waking up the CPU. System support ASICs can help with the pin settings under system software control.

Internal power-management logic looks for inactive blocks and turns them off until needed. The logic also monitors the instruction stream by observing resources not being called and turning them off, which is basically a form of dynamic power management. This is possible because the circuits are implemented with fully-static CMOS logic. Consequently, the expected power drain should average about 1 W.

Both the 601 and 603 have a three-issue superscalar architecture that tries to execute three of four possible operations every cycle. The processor can execute an integer, load-store, floating-point, or branch operation (in the 601, the load-store was part of the integer unit; in the 603, it's a separate element in the CPU architecture). Since the 603 wasn't intended for high-end systems, it lacks the full multiprocessing support on the bus interface. However, snooping is done on the data cache.

Designers at IBM and Motorola have already fabricated first silicon and placed a limited number of samples into the hands of first-tier customers. Details of the processor were unveiled last month at the Microprocessor Forum conference held in Burlingame, Calif. Commercial samples should be available in the first quarter of 1994. Contact Russell Stanphill at Motorola, (512) 891-2000; or Robert Mansfield at IBM, (512) 823-0842.

DAVE BURSKY



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ADVANCED DSP-BASED SPEECH RECOGNITION COMES TO THE PERSONAL COMPUTER

In less than a year, a speech-recognition system will be available that could revolutionize the way PC users input their data. Based on a DSP architecture, it will be capable of maintaining 32,000 active words, a vocabulary that's large enough to handle most word-processing applications.

Most of today's real-time speech-recognition systems come with trade-offs. PC-based systems usually have a limited vocabulary. And those that possess a large vocabulary (in the thousands of words) can only keep a limited number of words active at a time. For example, the system might hold 10,000 words. But each application is associated with 100 words, and only those words would be used with that application. For instance, a spreadsheet would have access to such words as file, save, retrieve, move, copy, edit, find, and so on.

Another limitation is the speed in which words can be input. Today's PC-based speech-recognition systems can only be used for single words or short word combinations, not for dictation. The way around these limitations is to use a high-powered computer, such as a mainframe or supercomputer. However, even though these recognition systems are powerful enough to handle extremely large vocabularies at the speed of normal speech, they're quite expensive.

The Desktop Dictation system, a software-based solution from IBM, is certain to change this scenario. It's based on a plug-in card with a proprietary 22-MIPS DSP chip specifically developed for speech recognition to hasten computations. The DSP IC offloads a significant portion of the cycle-intensive acoustic preprocessing and statistical matching from the host CPU (about 70% of the cycles).

The Desktop Dictation system is a derivative of an earlier product, the Speech Server, which is only available on RISC servers. For the first time, IBM ported its high-end algorithms to a PC-based product, which can run on a 486-class PC under the OS/2 operating system and should sell for less than $1000.

"The system is capable of running in an all-software environment. We believe that on a Power PC- or Pentium-based system we may be able to get by without the DSP circuit. But on a 486-class machine, we need the extra horse power," says Elton Sherwin, manager of IBM's speech-recognition strategy. In addition, the multiprocessing capabilities of OS/2 help make speech recognition possible.

When the system hears a word, it does some preprocessing based on the word's acoustics. Then, it does a "facts match" to the 100 to 300 words in the dictionary of 32,000 that most closely match the spoken word. For example, in a sentence that starts with the word "to," it would locate a number of words that sound like "to." Then it performs a statistical analysis to estimate what the correct word is by looking at the preceding and following words. After a selection is made, the system tries to predict what words will follow.

For example, assume that the letters "t" and "o" were displayed, and the next word is "many." The system goes through its iterative process, but now there's some context to use. After seeing the word "many," the system can go back, and through a statistical-probability analysis of the neighboring words, it realizes that the preceding word should be "too," not "to." If "to" was instead followed by a word such as "men," it would have been changed to "two."

There is no predefined limit as to how many words the system will analyze before and after, but the average is three. If the statistical match is poor, it will go back further and run through more combinations. Even while the search is occurring, the system listens for and does computations on the next word, an attribute of its multitasking capabilities.

The recognition system is user-dependent. This means that it must be trained to the user's voice, which takes about 90 min. IBM currently offers a user-independent system that requires no voice training, but its vocabulary is limited to about 1000 words.

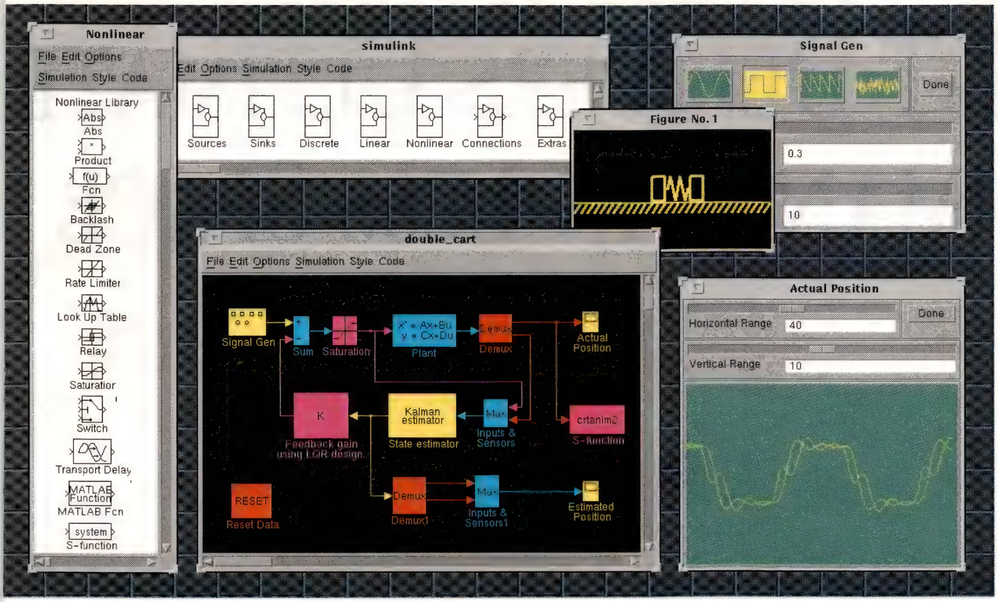
In the training session, the user repeats all of the base phonemes of the language in different uses (the English language consists of 53 base phonemes). All 32,000 words needn't be repeated because the system builds a series of statistics for the user's voice using the phonemes. Then, those sounds can be mapped to all of the words in the active vocabulary.

If a spoken word isn't recognized, the statistical model can adapt by retaining the context of how the word is used. This is needed because many people make up their own meanings for words, especially in slang or with proper names. For example, "Electronic Design magazine" is a difficult phrase to analyze because Electronic and Design typically aren't used as proper names. The first time you correct and capitalize the two words, the system will realize that a correction was made. Then it will trap that correction and store it for any future occurrences.

Words can be added to the vocabulary either beforehand or on-the-fly. There are some difficult phrases where what's spoken is portrayed differently on the screen. An example is IEEE—most people don't say I-E-E-E; they say I-triple-E. This type of word or phrase is entered in a special field that permits the system to override a phonetic pronunciation. Most of these special cases involve abbreviations or acronyms.

The 32,000-word system requires about 6 to 8 Mbytes of system RAM to operate correctly. In addition, the vocabulary takes up about 20 to 30 Mbytes of hard-disk space. The system works with any program running under OS/2, including Windows 3.1 applications. The DSP card will be available from IBM in both ISA and Micro Channel bus configurations.

RICHARD NASS



Simulating a system with SIMULINK: Scope block and MATLAB animation window show results while the simulation is running. You can change parameters during a simulation to do "what if" analyses.

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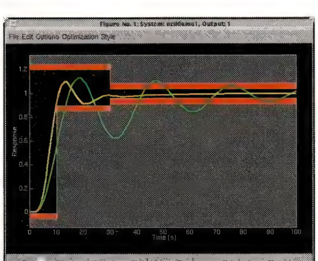

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WITH AN ARCHITECTURE TUNED TO GRAPHICAL USER INTERFACES, THE WINDOW RAM SPEEDS DATA TRANSFERS WITH MINIMAL SILICON OVERHEAD.

DUAL-PORT DRAM ACCELERATES WINDOWS

DAVE BURSKY

Now that almost every desktop and portable computer system typically comes with a graphical user interface (GUI), display subsystems have developed into somewhat of a performance bottleneck when trying to achieve responsive systems. Video RAMs have become key components in high-performance video subsystems by improving bandwidths, which in turn accelerates data speed. But their high silicon cost, which is typically 100% or more than that of standard DRAMs, limits them to being used in only the highest-performing graphics subsystems.

Employing some VRAM-architecture ideas but altering the way data is manipulated and directed has spurred on the creation of a new type of video memory—the Window RAM (WRAM). Developed by Samsung Semiconductor, the optimized memory architecture handles the types of operations typically encountered in a window-based GUI. Yet the memory can be implemented much more efficiently than the VRAM (smaller chip area and thus lower cost) and still deliver five times or better performance levels.

The use of GUIs poses several challenges to graphic subsystem designers, one of which is how to display more information on a screen without flicker. These diametrically opposed challenges add to system overheads because larger frame buffers will be needed, and larger buffers require higher bandwidths to transfer all of the video information within one frame period. However, such needs run counter to the needs of system manufacturers, who want to reduce system costs to stay competitive.

The dual-ported 256-kword-by-32-bit WRAM addresses all of these concerns. It does this by providing VRAM-like performance at close to DRAM prices. To do that, designers at Samsung Semiconductor made the KM4232C256 as complete as possible, effectively implementing a 1024-by-1024-pixel by 8-bit frame buffer on one chip *(Fig. 1)*.

Wide internal buses in the memory permit data transfer between subsections at rates of up to 1.6 Gbytes/s. That allows rapid fill, text move, scroll, and block-move operations. To

enhance block transfers for Windows-based applications, the WRAMs also include a block-write mode of eight columns, which allows a transfer of 32 bytes at a time to take place.

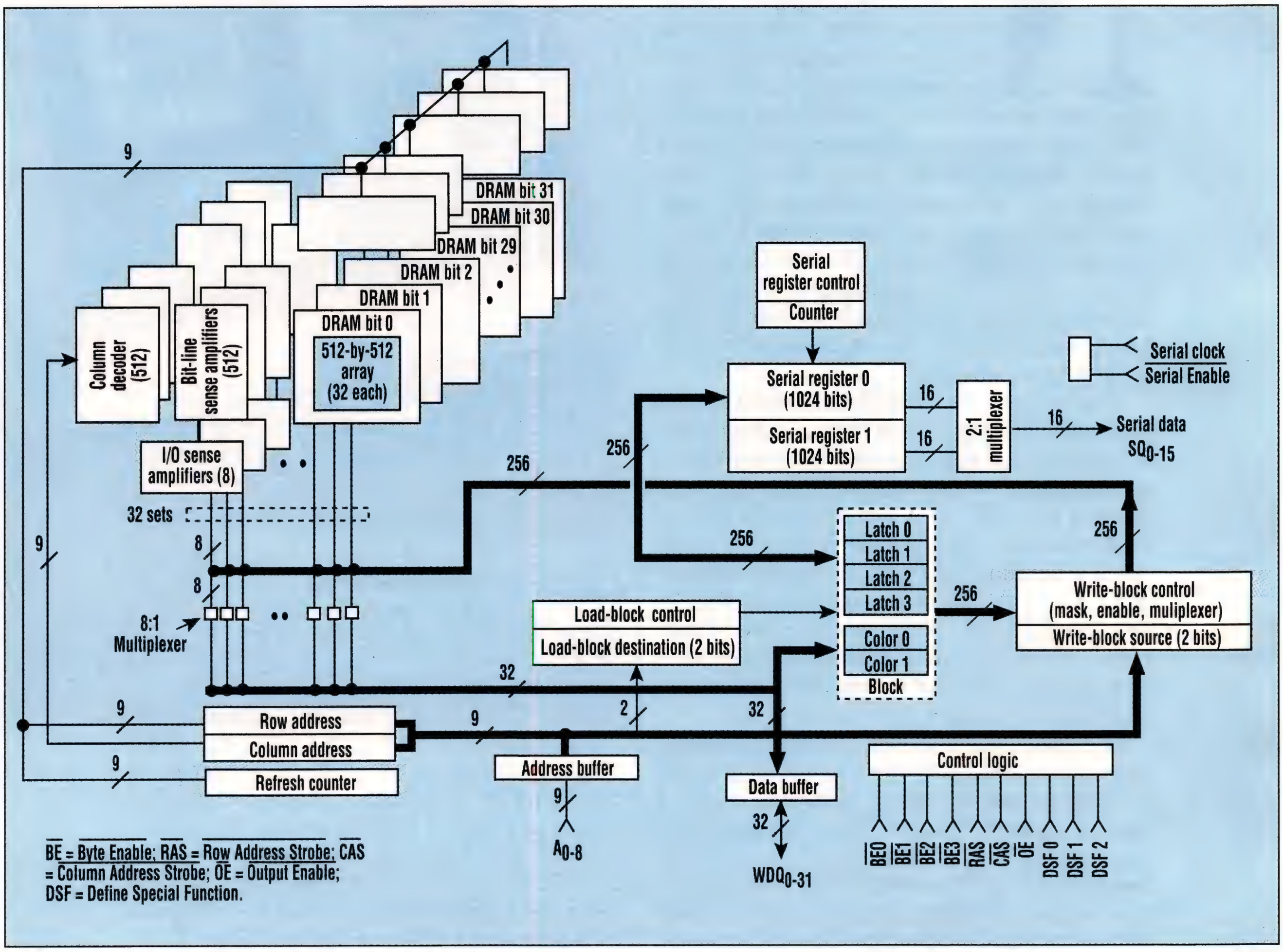
Fabricated with Samsung's 0.5-μm CMOS twin-well process (the same process the company uses for its 16-Mbit DRAMs), the WRAM will come in versions for 5- or 3.3-V operation. The 5-V version (KM4232C256) will have TTL-compatible I/O levels while the 3.3-V unit (KM4232V256) comes with low-voltage TTL-compatible I/O lines. When operating at 5 V and at maximum speed (60-ns access time, 20-ns ultra-fast page mode), the WRAMs consume 200 mA, while the 3.3-V versions draw 180 mA maximum. On standby, the WRAMs draw just 8 mA.

To compare VRAM capabilities with the WRAM, let's take a quick look at a 1-Mbyte frame buffer built with conventional VRAMs and the 1-Mbyte WRAM. Such a system can deliver video bandwidths ranging from 266 to 1600 Mbytes/s, depending on the memory depth and organization *(Table 1)*.

Among the bus widths and block sizes compared by Samsung Semiconductor's designers was a theoretical 8-Mbit VRAM option. In the overall comparison, the highest bandwidth achieved by the VRAMs was about 800 Mbytes/s, assuming the page cycle stays at 40 ns. The 20-ns page cycle of the WRAM, however, lets the frame buffer deliver data at twice the rate of the VRAMs.

In a scroll example using just the WRAM, the sequence of operations to perform the scroll includes just eight instructions—four to load the internal latches from the RAM array, and four to transfer the latch contents back to the RAM array *(Table 2a)*. The first latch transfer requires 60 ns; the remaining seven transfers need just 20 ns each. As a result, just 200 ns are needed to move 128 bytes of data, which translates into a memory bandwidth of 640 Mbytes/s.

Performing aligned block moves is equally fast: Just transfer data from the memory to the latches and then read the data back from the latches into a new location *(Table 2b)*. Only 320 ns are needed to move 128 bytes of data, which translates into a transfer speed of 400 Mbytes/s. Additional performance numbers include 10-pixel vector drawing at 4.1 Mvectors/s, 7-by-9-pixel character draws at 4.5 million characters/s, and bit-block transfers at a rate of 640



1. PACKING THE EQUIVALENT of a complete 1-Mbyte frame buffer on a single chip, the Window RAM designed by Samsung Semiconductor simplifies graphic subsystem design and improves frame-buffer bandwidth. On-chip 256-bit-wide buses can transfer wide data words from the memory array to the serial output registers, or to the four data latches, in just a few memory cycles. The split serial-memory registers allow continuous data streams to be delivered over the 16-bit video port.

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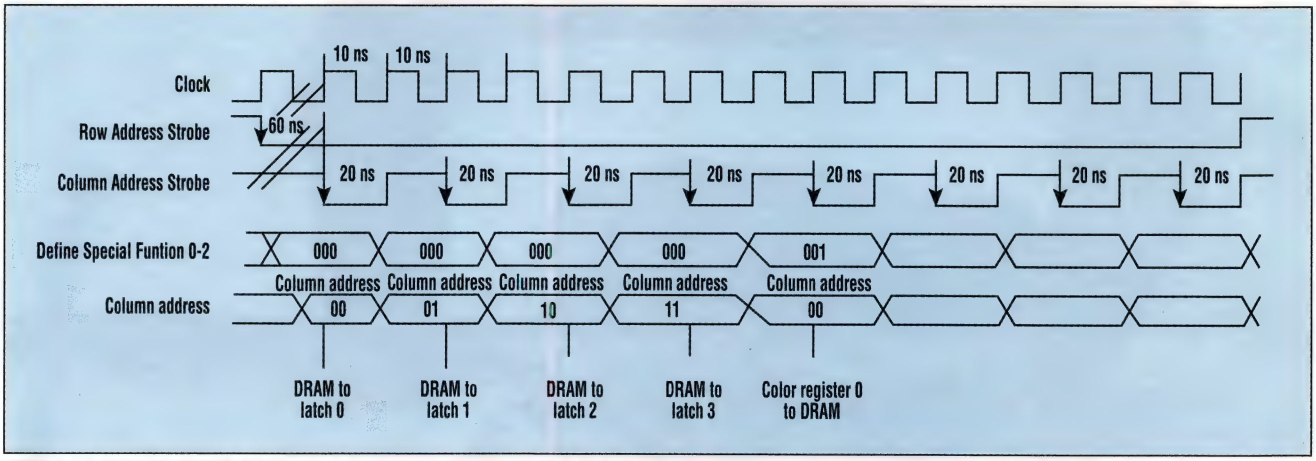

2. AFTER THE FIRST ACCESS, WHICH TAKES 60 ns, subsequent transfers from the DRAM array require just 20 ns apiece. Each cycle permits the transfer of 256 bits (32 bytes) into the memory (from the internal registers), or from the memory to the internal latches or serial register.

Mbytes/s.

On the host-port side, the WRAM looks very similar to a conventional DRAM except for a super-pipelined fast-page mode that operates at 20 ns per transfer. Consequently, the host interface to the CPU can transfer data at 200 Mbytes/s (32 bits wide, 50 Mtransfers/s) using its "ultra-fast" page mode, or 60 ns for a standard random-access request. Thanks to the 32-bit-wide transfers and the ultra-fast page mode, window Save and Restore operations are quite fast.

The video port delivers streams of 16-bit-wide words in a word-serial fashion, much like standard VRAMs. But unlike VRAMs, data can only be transferred out of the port, thus simplifying the I/O structure. VRAM serial-data ports were designed for bidirectional operation, which also suits the chips to being employed in non-graphic data-transfer applications.

The WRAM's internal memory array is organized as 32, 512-by-512-bit planes and is connected through a wide 256-bit bus to the rest of the chip's logic. The bus is multiplexed down to 32 bits for the host side's random-access data port. However, the 256-bit-wide bus is maintained to tie into the two 64-word-by-16-bit serial registers that feed the 16-bit word-serial video port through a 2:1 multiplexer. By loading one register and starting the shift process, the second register can be loaded during the shift process. That second register can then be automatically swapped with the first register to ship its data out once the first register runs out of data.

The 256-bit-wide internal bus makes it possible for each 64-word register to be loaded in just four cycles. That leaves plenty of time for the shifter to finish emptying the other register before switching. Data from the memory array can be routed either to the serial registers, or to a special data-latch block that holds four 256-bit words. There are two 32-bit color registers, one for foreground and one for background color. A second register block on the chip contains two 32-bit registers that hold the write-block control bits for plane and true byte masking.

To handle the 16- and 32-bit data ports and allow for next-generation expansion, Samsung designers decided to put the WRAM into a 120-lead plastic quad-sided flat package. In addition to the nine multiplexed address pins and the 32 data lines, the host port includes a standard complement of active-low control pins—four byte-enable pins, an output enable pin, row- and column-address-strobe ($\overline{RAS}$ and $\overline{CAS}$) lines and three define-special-function (DSF) pins. The serial port side includes the 16-bit data port, a serial-clock line, and a serial-enable pin.

The three DSF pins along with the falling $\overline{CAS}$ line determine the WRAM's internal operation. The choice of mode can be changed on the fly. As a result, the user can change

TABLE 1: FILL TREND/PERFORMANCE COMPARISON FOR A 1-MBYTE FRAME BUFFER

Density	No. of pins per device	No. of devices	External bus width	Bytes/ block write	Page cycle	Bandwidth
Conventional VRAMs						
256 kbit	4	32	128 bits	0	60 ns	266 Mbytes/s
1 Mbit	4	8	32 bits	16	60 ns	266 Mbytes/s
1 Mbit	8	8	64 bits	32	60 ns	533 Mbytes/s
2 Mbit	8	4	32 bits	16	40 ns	400 Mbytes/s
4 Mbit	16	2	32 bits	32	40 ns	800 Mbytes/s
8 Mbit*	32	1	32 bits	32	40 ns	800 Mbytes/s
Window RAM						
8 Mbit	32	1	32 bits	32	20 ns	1600 Mbytes/s

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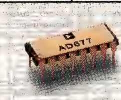

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operations quickly, even within the ultra-fast page mode. With all three DSF lines at logic 0, the two lower bits of the Column-Address pins at the falling $\overline{CAS}$ signal determine which of the four data-latch registers is loaded with a word from the DRAM array *(Fig. 2)*.

A state of 011 on the same DSF pins sends data from the latches back to the DRAM array. Other patterns on the DSF pins load or read the color and mask registers, switch color registers to change the background and foreground colors, transfer the color-register contents into the RAM array, set the serial-register shift pointer, perform the split-read transfer, and control the ultra-fast page read or write cycles.

With the on-chip quadruple 256-bit-wide data latch, background data transfers can occur inside the WRAM while data is being transferred out of the serial port or as the host port is being accessed. For instance, the host interface would first initiate a data transfer into one of the serial registers and start the transfer. Then, while data is being clocked out, additional words from the RAM array would be loaded into the latch and subsequently transferred back to a new location in the RAM array. Finally, before the serial register finishes its shifting operation, the other serial register is loaded with the proper data.

Thus, block moves, scrolling, and other data-movement operations take place with no apparent delays because the next lines of data can be rearranged in the memory while the current line is being transferred. This "background" transfer capability eliminated the need for large on-chip serial registers. Most of today's 4-Mbit VRAMs have large serial I/O registers, which include at least 512 bytes of serial-register storage. On the other hand, the WRAM trims the storage size by 50%, half the storage capacity by employing only two 64-word-by-16-bit registers. That reduces the chip area significantly, which in turn keeps chip cost lower than that of a VRAM.

TABLE 2B: DEFINING THE BLOCK-MOVE OPERATION

		RAS		CAS			
Cycle	Mnemonic	Address	Data	Address 9-4	Address 3-0	Data	Cycle time
Pipe read to block	URWL	S. row	WPBM	S. col. 0	Latch 0	x	60 ns
Pipe read to block	URWL	x	x	S. col. 1	Latch 1	x	20 ns
Pipe read to block	URWL	x	x	S. col. 2	Latch 2	x	20 ns
Pipe read to block	URWL	x	x	S. col. 3	Latch 3	x	20 ns
Pipe block write	UWC	D. row	x	D. col. 0	Latch 0	Clip L	60 ns
Pipe block write	UWC	x	x	D. col. 1	Latch 0	Clip R	20 ns
Pipe block write	UWC	x	x	D. col. 1	Latch 1	Clip L	20 ns
Pipe block write	UWC	x	x	D. col. 2	Latch 1	Clip R	20 ns
Pipe block write	UWC	x	x	D. col. 2	Latch 2	Clip L	20 ns
Pipe block write	UWC	x	x	D. col. 3	Latch 2	Clip R	20 ns
Pipe block write	UWC	x	x	D. col. 3	Latch 3	Clip L	20 ns
Pipe block write	UWC	x	x	D. col. 4	Latch 3	Clip R	20 ns

RAS = Row Address Strobe; CAS = Column Address Strobe; S. row = source row; S. col. = source column; D. row = destination row; D. col. = destination column.

Results: 320 ns to move 128 bytes; 400-Mbyte/s maximum throughput.

High Performance

With upcoming multimedia applications, more bits per pixel will be needed to improve the color images. Applications with 16 or even 24 bits per pixel will be commonplace even on home computers in the near future. The high color content in addition to megapixel display requirements will place a strain on today's graphics subsystems, which is why the VRAMs will be needed to deliver high performance at moderate cost.

A typical high-end subsystem with a 1280-by-1024-pixel display refreshed at 72 Hz and using true color (24 bits/pixel) requires a data transfer of 284 Mbytes/s to keep the screen refreshed. Allowing for additional system overheads that add, say, another 75 Mbytes/s of bandwidth requirements, puts the frame-buffer bandwidth requirement at 359 Mbytes/s. And that doesn't include system commands, arbitration overhead, and other factors that can further double the bandwidth requirement. Such high-bandwidth needs are hard to meet without VRAMs, and impossible to meet at the cost levels associated with DRAMs and the competitive PC market. That combination demands the performance of the WRAM at price levels close to DRAMs.□

TABLE 2A: CHARACTER-SCROLLING PERFORMANCE

		RAS		CAS			
Cycle	Mnemonic	Address	Data	Address 9-4	Address 3-0	Data	Cycle time
Pipe read to block	URWL	S. row	WPBM	S. col. 0	Latch 0	x	60 ns
Pipe read to block	URWL	x	x	S. col. 1	Latch 1	x	20 ns
Pipe read to block	URWL	x	x	S. col. 2	Latch 2	x	20 ms
Pipe read to block	URWL	x	x	S. col. 3	Latch 3	x	20 ns
Pipe block write	UWC	x	x	D. col. 0	Latch 0	Clip	20 ns
Pipe block write	UWC	x	x	D. col. 1	Latch 1	Clip	20 ns
Pipe block write	UWC	x	x	D. col. 2	Latch 2	Clip	20 ns
Pipe block write	UWC	x	x	D. col. 3	Latch 3	Clip	20 ns

RAS = Row Address Strobe; CAS = Column Address Strobe; S. row = source row; S. col. = source column; D. col. = destination column.

Results: 200 ns to move 128 bytes; 640-Mbyte/s maximum throughput

Price And Availability

Samples of the KM4232C256 window RAM will be available in the first quarter of 1994. In lots of 10,000, the 5-V version of the WRAM will sell for $31.00 each. The KM4232V256 3.3-V version of the WRAM will also go for $31.00 each in the same quantities. All parts will be available as engineering samples by the first quarter of next year. Production quantities will be available by the fourth quarter of 1994.

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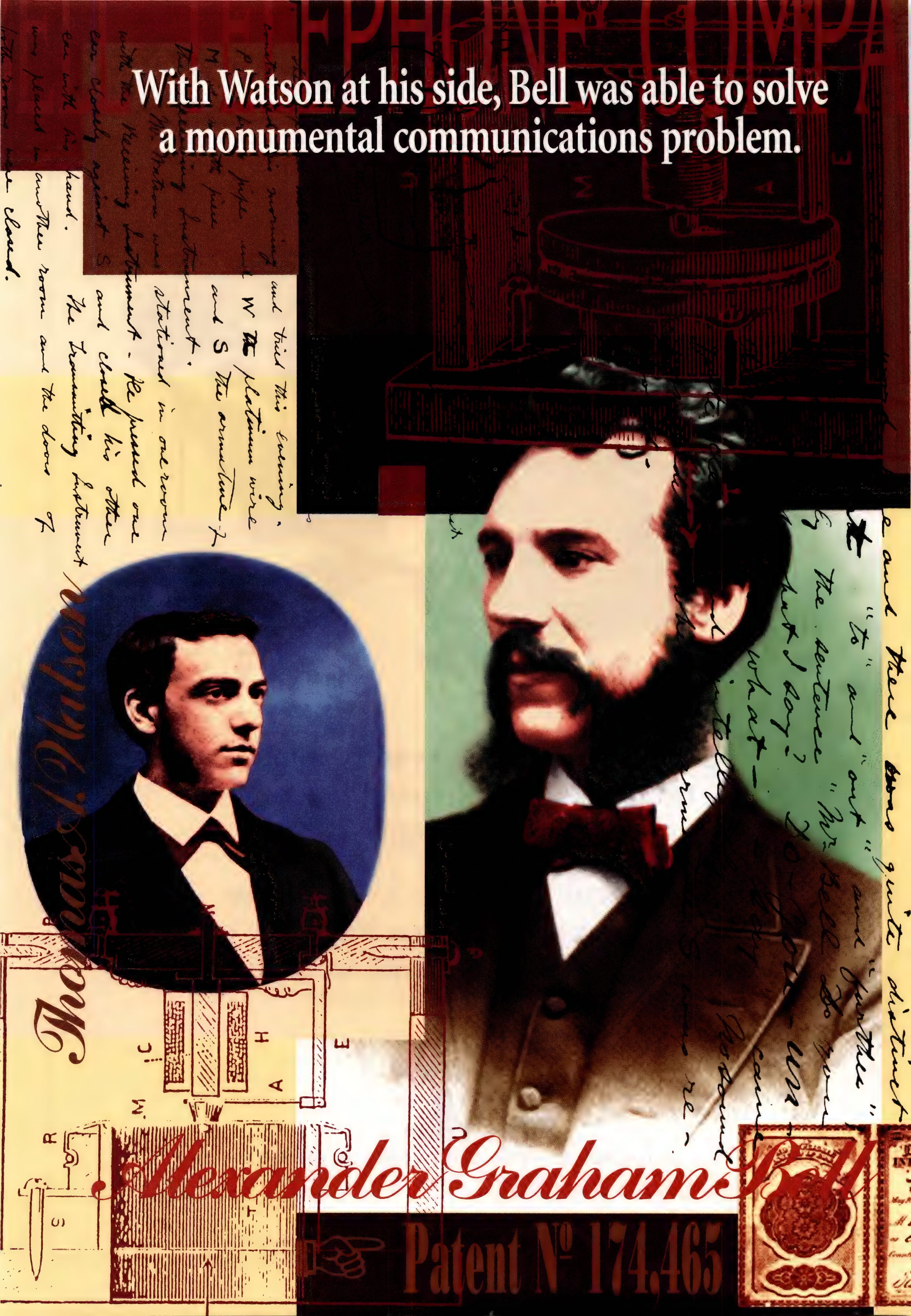

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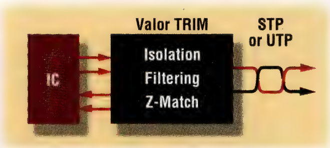

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[1] SD6020 denotes a surface-mount package.
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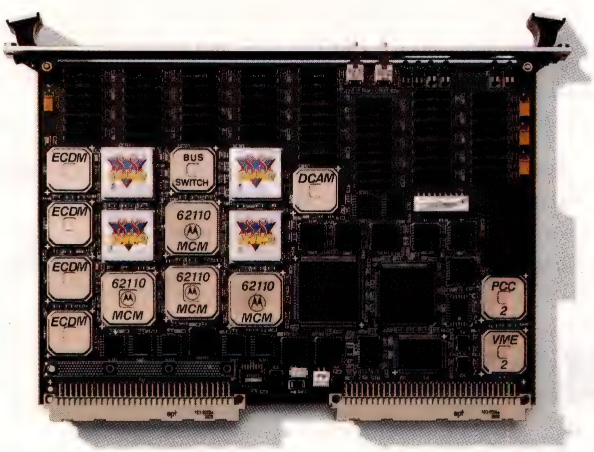

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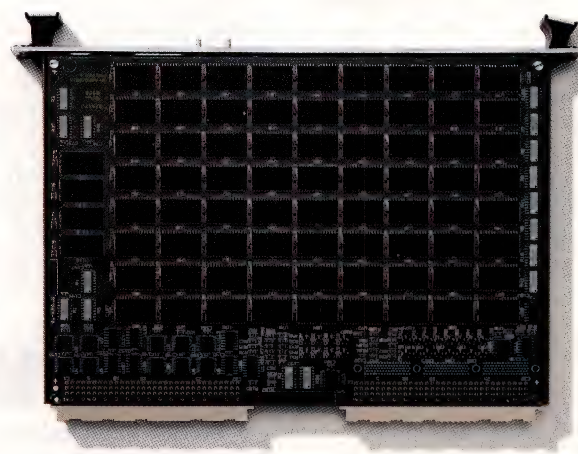

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DIGITAL AUDIO DELIVERS NON-STOP INNOVATIONS

Speech And Music Keep Pushing The Frontiers Of Computing Across Technologies Including Compression, Synthesis, And Speech Recognition.

BY JACK SHANDLE

Digital audio is already playing to rave reviews among engineers who design PCs, workstations, and consumer appliances. But their enthusiasm is only likely to grow as new markets emerge from the synthesis of existing ones. In the beginning, audio on personal computers was practically synonymous with computer games and entertainment. But in the future, business-oriented products will routinely integrate speech-oriented functions that include text-to-speech, speech recognition, and telephony. Entertainment-oriented products will add music synthesis, and some music will even find its way into the workplace by riding multimedia.

As digital audio becomes more pervasive, specific technologies have emerged as critical design problems. These include audio compression, synthesis, and speech recognition. Today's technologies—algorithms and hardware—are being supplanted in quick order by more powerful technologies. It's only a matter of time before virtually every engineer will come in contact with them.

Digital audio starts by digitizing analog audio signals using a three-step process. First, the analog source audio from a microphone or line-level input is digitized using analog-to-digital converters. Second, the digital data is sampled in the time domain in a way to approximate the original analog waveform. Third, the sampled, digital data is recorded on some medium: CD, tape, or hard disk. During the sampling process, both the sampling resolution and the sample rate have an impact on the quality of the digitized sound. The resolution determines the signal's dynamic range. In musical terms, this means the range between the softest and the loudest sounds that can be reproduced. A sample with 8-bit resolution, for example, has 48 dB of dynamic range. Similarly, a 16-bit sample provides 96 dB of dynamic range, which is equal to the quality of an audio CD disc.

The sampling rate, on the other hand, primarily determines the range of frequencies that can be faithfully reproduced. This frequency response has a theoretical limitation set by the Nyquist theorem: frequency response equals one-half the sample rate. A 44.1-kHz sampling rate—the sampling rate of CD recordings—delivers a frequency response of 22 kHz, which covers the dynamic range of the human ear. More samples require more memory to store them. While it's understandable that sampling rates will vary to accommodate the trade off between desired quality and storage limitations, there are also variations from computer platform to platform *(see the table)*.

WAVE-TABLE SYNTHESIS

FM synthesis, invented at Stanford University, was the first sound synthesis technology. It's based on constructing complex sounds by combining simple audio waveforms. Although the technology is capable of simulating many instruments and sound effects, the music it creates tends to be tinny and somewhat fuzzy. Clearly, fm synthesis leaves plenty of room for improving the quality of the sound produced.

Although fm synthesis leaves something to be desired in terms of quality, it is an inexpensive technology to integrate into a system. For an additional

TABLE: POPULAR AUDIO SAMPLING RATES

Rate	Comments
5.5 kHz	One-fourth the Mac sampling rate.
7.333 kHz	One-third the Mac sampling rate.
8 kHz	A telephony standard that's compatible with μ-Law and A-Law encoding.
11.025 kHz	One-fourth the CD sampling rate and one-half the Mac sampling rate.
22.050 kHz	The MAC and SoundBlaster (as used in PCs) sampling rates.
32 kHz	Used in digital audio and TV; some DAT machines support it.
44.1 kHz	The CD sampling rate.
48 kHz	The DAT (Digital Audio Tape) sampling rate.

cost, however, users can achieve significantly higher quality with wave-table technology. Wave-table synthesis is today's state-of-the-market technology for music synthesis. It takes its name from the tables of waveforms that store specific sounds. Instead of trying to create a musical note by combining a few frequencies, as is done is FM synthesis, the actual sounds of instruments are sampled and stored in ROM. Although the sound quality is very high, wave-table synthesis typically requires a great deal of ROM—2 or 4 Mbytes is not uncommon even with clever conservation techniques, and this involves added costs.

The primary means of keeping wave-table memory requirements under control is by taking bites of sound—just enough to define a specific note played on a piano, for example—and then processing the bites in real time during playback. A short sample of a note played continuously in a loop simply prolongs the duration of the note. These samples, along with the parameters that control the playback, are often called patches, a term that harks back to the original synthesizers that used patch chords to stitch sounds together.

Three other unfamiliar terms encountered in audio-synthesis technology are polyphony, multisampling, and multitimbral. Polyphony is the ability to play multiple notes simultaneously. A synthesizer with 16-voice polyphony can play 16 unique pitches at the same time. Changes in pitch are created from sampled sounds by changing the playback rate. Multiplexing circuitry is used to read a sample and play it back at different rates simultaneously without requiring unique samples and digital-to-analog converters for each note. As a result, the synthesizer can play chords or any other passage that requires more than one note sounding at a time.

MULTISAMPLING

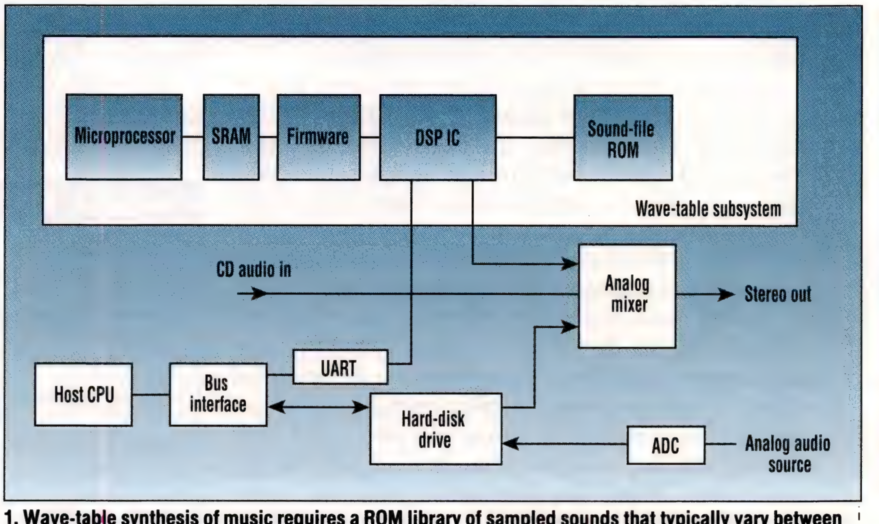
Multisampling refers to the technique of taking samples of an instrument's range at various intervals (every third note is one common interval) to reduce the artifacts that occur when samples are interpolated by large changes in scale. Multisampling captures the evolution of the original instrument's timbre (the quality given to a sound by its overtones) over its original range.

In addition, digital synthesizers can be compared on the basis of how many different instruments they can play simultaneously, which is also referred to as their multitimbral capability. Ideally, the multitimbral capabilities match the level of polyphony so that any voice can play any available timbre. A device with 32 multitimbral voices can play sound from 32 different instruments simultaneously.

Wave-table synthesis almost invariably involves the Musical Instrument Digital Interface (MIDI) protocols *(see "General MIDI creates order from the chaos of music-synthesizer hardware," p. 56).* MIDI provides a standard for indexing stored sounds so that a trumpet sound used in one synthesizer to create a composition can be played on another synthesizer. Although MIDI was the beginning of a standard for playback, the various early synthesizer manufacturers had different flavors of MIDI. That incompatibility problem was resolved in 1991 with the adoption of a General MIDI format that synthesizer manufacturers comply with when making cards for personal computers. A further refinement, first available in early 1993, is the Roland General Synthesizer enhancements to General MIDI. The enhancements include sound variations, reverb, and chorus effects.

One of the technology leaders in wave-table synthesis is E-mu Systems Inc., Scotts Valley, Calif. E-mu leaped to the fore with its Proteus products, which are used both in proprietary studio-grade synthesizers and, more recently, as add-in cards for personal computers. E-mu's synthesizer—and most of its competitor's products—consists of three primary components: ROMs that store the sound samples comprising the instrument library; a proprietary chip based on a digital-signal processor that mixes and combines the samples; and firmware that defines the types and extent of processing the chip will execute *(Fig. 1).*

In addition to its own hardware solution, E-mu licensed its instrument library to AT&T Microelectronics for integration into AT&T's Multimedia Module Library. This allows hardware developers to use AT&T's DSP32xx family of digital-signal-processing (DSP) ICs and their VCOS operating system. Regardless of whether the processing is



1. Wave-table synthesis of music requires a ROM library of sampled sounds that typically vary between 2 and 4 Mbytes. Firmware describes the types of functions that can be utilized. An application-specific or general-purpose digital-signal processor executes the firmware commands on the library sounds, and a microprocessor orchestrates the procedures.

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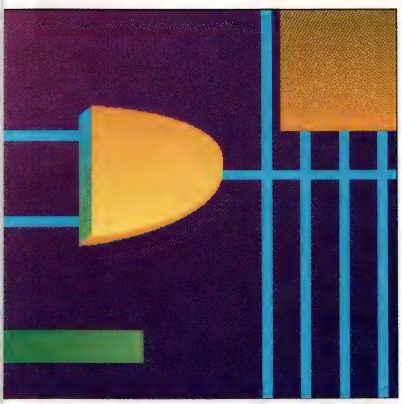

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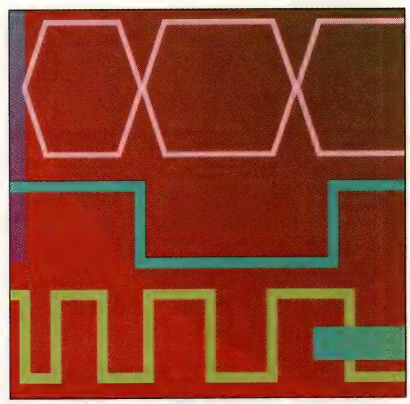

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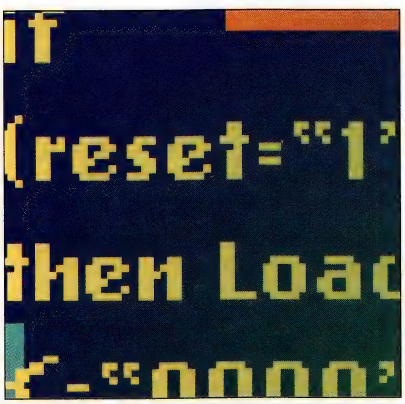

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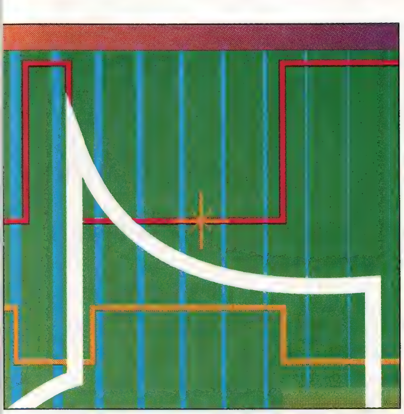

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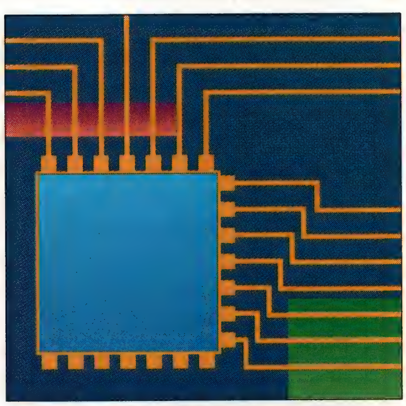

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done on a proprietary chip or a general-purpose DSP IC, roughly the same type of processing is executed. Faster processors can provide more voices, or polyphony.

Other functions of the Proteus products include gain control, filtering, and enveloping. Firmware can be used to define low-frequency oscillators to create vibrato, tremolo, and other effects. Two firmware-definable envelope generators per voice generate dynamic responses to notes when the notes are initiated. The envelopes, which handle volume, pitch, and crossfading between sounds, are controlled in six segments that mimic the playing of an actual instrument: delay, attack, hold, decay, sustain, and release.

Two low-frequency oscillators per voice are used in the E-mu architecture as modulators to produce vibrato when routed to pitch or tremolo when routed to volume. Five wave shapes are available to modulate the low-frequency oscillators.

As might be expected, one of the major differentiating characteristics of competing sound cards that use wave-table synthesis are the samples of sounds themselves. E-mu, for example, has a library of "every instrument known to man" in 16-bit, 44.1-kHz CD-quality samples. A relatively high-end card, however, would deliver sound samples containing over 200 instrument waveforms stored in 4 Mbytes of ROM.

Waveguide Synthesis

The large file sizes required to synthesize high-quality music using wave-table technology are hindering its implementation on cost-sensitive personal-computer platforms. The next new synthesis technology, digital waveguide technology, should go a long way toward solving that problem.

Waveguide technology shifts the focus from sampling the sound created by instruments to creating models of the physical instruments them-

GENERAL MIDI CREATES ORDER FROM THE CHAOS OF MUSIC-SYNTHSIZER HARDWARE

Since 1991, the Musical Instrument Device Interface (MIDI) has moved from being strictly an electronic-musical-keyboard technology to becoming a widely accepted standard in desktop computing. It's supported by the DOS-Windows, Apple Macintosh, and most workstations.

MIDI messages don't contain sound. Instead, they're instructions that tell a music synthesizer which notes to play, how loud to play them, and the instrument should be emulated.

As defined by the MIDI 1.0 Specification, the data stream is a 31.25-kbit/s, unidirectional, asynchronous bitstream that transmits 10 bits per byte (eight data bits, one start bit, and one stop bit). The data stream is generated by a MIDI controller, which could be a musical instrument keyboard or a MIDI sequencer, a device that captures, stores, edits, and combines MIDI sequences. MIDI messages are interpreted into sound by a sound generator.

Although many types of MIDI messages exist, most of the information in a data stream is transmitted as channel-voice messages. These consist of a status byte and one or two data bytes. The status byte includes a 4-bit channel address that directs it to the proper MIDI channel of the 16 channels available. The first data byte indicates the key to be turned on and the second indicates velocity, which is used to control the sound's amplitude.

The ability of a sound generator to play more than one note at a time is called polyphony. Polyphony is specified as a number of notes or voices. The current generation of sound generators typically have 16 or 24 voices. Those sounds can be referred to as patches, programs, algorithms, or timbres.

Sounds are created by specifying specific program or patch numbers. A synthesizer or sound generator is referred to as being multitimbral if it can produce different types of sounds simultaneously. For example, a synthesizer that has 24-voice polyphony and is six-part multitimbral could synthesize a six-piece band.

Two important amendments to the MIDI specification are General MIDI, which simply standardizes the patches in the MIDI index for cross-synthesizer compatibility, and the Roland General Synthesizer functions. The Roland GS functions are a superset of General MIDI. They include all of the General MIDI sounds and add new sounds that are variations of General MIDI sounds. Also included are adjustable reverb and chorus effects.

The de facto-standard for MIDI-interface add-in cards for PCs is the Roland MPU-401 interface. It's a smart interface that also supports a simple pass-through mode known as UART (universal asynchronous receiver/transmitter). Most MIDI software uses only the UART mode.

Other important standards for MIDI are the Windows 3.1 and MPC (Multimedia PC) specifications. Both use General MIDI patch definitions and include 128 patches for melodic instruments and sound effects, plus 46 percussion sounds. MPC-compliant audio adapter cards must have MIDI in and out.

Windows 3.1 is shipped with drivers for the MPU-401 and the Roland LPC-1, which integrates the MPU-401 interface with the Linear Additive synthesizer used in the Roland MT-32 sound module. The multimedia extensions to Windows specify the MIDI channels that are to be used for MPC-compatible MIDI files. Channels 13 through 16 are used by base-level synthesizers. Advanced synthesizers with more polyphony use channels 1 through 10.

selves. It holds the promise of creating the highest possible synthesis because the instrument model can be modulated with the same parameters as the real instrument.

Past attempts at physical modeling have been unsuccessful because the techniques were based on numerical integration of the wave equation for each instrument. This approach implies a very high computational load, because at least one multiplication and/or addition is required for each point on a three-dimensional grid that's set up within the instrument. Theoretically, spacing for each point in the grid must be less than half the wavelength of the highest audio frequency that can be attained by the instrument. This kind of brute-force numerical solution led to the creation of prohibitively expensive synthesis algorithms.

Waveguide technology, on the other hand, pursues a different path. The generalized physical description of a waveguide is simply a tube through which waves travel (or, a string along which waves travel). The tube is much longer than it is wide, and it resonates with frequencies determined by its dimensions. If the waveguide bends, changes diameter, or joins another waveguide, additional resonances are produced.

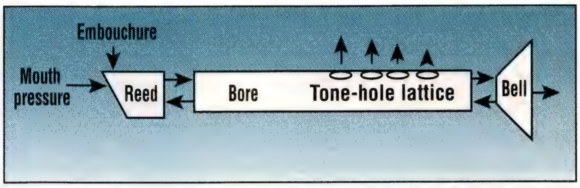
For example, the physical model of a single-reed woodwind consists of a reed, bore, tone-hole lattice, and bell *(Fig. 2)*. If the bore is cylindrical, as in a clarinet, it can be modeled using a bidirectional delay line. If, as in the case of a saxophone, it is conical, it can still be modeled as a bidirectional delay line but the interfacing is more complex. Because the primary control variable is air pressure exerted on the reed by the mouth and lips—an activity known as embouchure in the music world—pressure waves make the best waveguide variables.

SPLITTING ENERGY

The bell can be viewed simply as a crossover network that splits signal energy between woofers and tweeters in the loudspeakers. Tone holes can be treated in the same way with good results, but other recently developed models can easily be adapted to a traveling-wave formulation. The effect of the reed can be implemented as a single table lookup, or as a segmented polynomial evaluation per sample whose parameters are the difference between the mouth pressure and the incoming bore pressure. The player's embouchure controls damping of the reed, reed aperture width, and other parameters. All of these parameters can be implemented in lookup tables.

Waveguide theory has to a large extent been formulated by Julius Smith, a professor at Stanford University's Center for Computer Research. Stanford is also a hotbed of continuing research for modeling specific instruments. In fact, the Center recently licensed its technology to Media Vision, Fremont, Calif., and Yamaha Corp., Tokyo, Japan.

Waveguide synthesis uses mathematical models



2. The physical model of a single-reed woodwind used in waveguide synthesis incorporates a reed, a bore, a tone-hole lattice, and a bell. The player's mouth pressure and embouchure also come into play in creating the air pressure, which represents the fundamental waveguide variable. In general, instruments can be modeled as a bidirectional delay line that's influenced by the instrument's physical characteristics.

of waveguides and oscillators that behave in the same way as their real-world counterparts. "A clarinet, to a first approximation, is a cylindrical bore with a nonlinear oscillator (the reed)," says Perry Cook, a researcher at Stanford who is also on Media Vision's technical staff. "If you don't mess it up with things like tone holes, you can actually do a simulation of a clarinet with a fairly low computational budget."

Instead of calculating a physical variable, as physical models had done in the past, the wave equation for a particular instrument is first solved in a general way to obtain descriptions of traveling waves in the medium that produces the sound. These traveling waves are simulated in the digital model of the waveguide. The waves must be summed together to produce a physical output.

In the theoretical case of a lossless environment, a traveling wave between two points can be simulated using nothing but a digital delay line. In the real world of frequency dependent losses and dispersion, the losses and dispersion can be lumped at discrete points so that much of the simulation still consists of a lossless delay line. This is essentially why computational costs are so low in waveguide-synthesis algorithms.

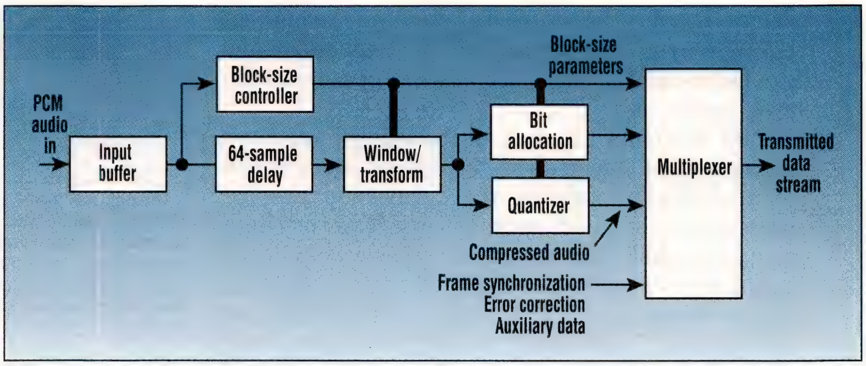
In software, a delay line can be implemented by a single fetch, store, and pointer update for each output sample. For a 500-sample-long delay line, the computational requirements of waveguide synthesis are 1000 times lower than attempting to solve the wave equation by brute force. As a result, several CD-quality voices can be sustained in real time on a single, low-cost DSP IC—as long as the physical models are kept relatively simple.

Waveguide synthesis will most likely utilize the MIDI protocols to interface with personal computers or electronic keyboards. These machines "create" the sound to be played by referencing a specific instrument and musical note in the MIDI index. An example of an instruction, says Cook, would be to call for a MIDI note from "a trombone playing middle C at a certain wind velocity."

Waveguide researchers must map specific delay-line lengths and other parameters into the standard MIDI index. Because MIDI doesn't provide for the detailed type of control possible with waveguide synthesis, it will require numerous extensions to accommodate the range of musical expres-

sions, says Cook. MIDI's architecture does, however, allow for these types of extensions.

Creating virtual instruments using waveguide technology is an ambitious undertaking. But Cook discovered that very good approximations can be found using a mathematical model of a meta-instrument that represents a particular family. One of the interesting characteristics of waveguide technology, he says, is that a virtual microphone can be placed anywhere inside the meta-instrument to record the sound.



3. Audio compression using the AC-2 algorithm created by Dolby Laboratories leverages the psychacoustical model of human hearing. Some of the key components include a block-size controller, which creates segments of digitized sound that vary in size according to the characteristics of the sound; a transform function that describes the sound in terms of a mantissa and coefficient; a quantizer that divides the information into subbands; and a bit-allocation block that assigns a specific number of bits in the data stream to describe the sampled audio.

In a somewhat surprising development, the audio characteristics of different instruments in the same family can be created simply by moving the virtual microphone to different locations in the meta-instrument. All of the brass instruments, jet-reed instruments (such as an organ), and cane-reed instruments (except for the saxophone) can be modeled this way with a wind meta-instrument patch, says Cook. That accounts for about 25 of the 125 instruments in the standard MIDI index. Similar results have been obtained with other families but the work is still incomplete.

Speech Compression

The basic principles of waveguide technology can be applied to human speech to accomplish high-quality speech encoding and playback with very high compression ratios—36:1 or greater. The fundamental model of how speech is generated includes a sequence of bursts of air from the lungs that are shaped by the throat, vocal chords, teeth, and tongue. "Changes (in the sound produced) do not occur at a rapid rate," says Asaf Mohr, vice president of the DSP Group Inc. Santa Clara, Calif., "so it is reasonable to use frames of one-thirtieth of a second."

Using a frame of that duration, the DSP Group's TrueSpeech algorithm models the shape of the human speech organs using digital-filter parameters and the amplitude of the air pressure being exerted by the lungs. The filter coefficients and other parameters are used to define the "shape" of the sound. The result is that one minute of speech can be compressed into 60 kbytes of digital storage instead of the nearly 1 Mbyte when using conventional techniques. The quality is virtually the same as with lossless compression using adaptive-differential, pulse-code modulation (ADPCM).

Modeling the organs of human speech is, however, only one aspect of the algorithm. Several attributes that distinguish human speech from other audio sources also contribute to the algorithm's robustness and compression efficiency. "For any given person at a given time," says Mohr, "there is low variability in pitch." Other attributes include the fact that the partitioning between sound and silence is meaningful (as in when someone stops to think), and the frequency range of speech is about 8 kHz. Environment also comes into play. Speech over a normal telephone line, for example, is bandlimited to 3.5 kHz and speech is usually accompanied by external noises, compared to a recording studio where background sound is virtually eliminated.

The TrueSpeech algorithm is also computationally efficient. It is asymmetrical, which in this case means encoding takes six times more computational horsepower than decoding. Using the Texas Instruments TMS32030 DSP IC for a hardware benchmark, the algorithm requires about 6 MIPS to encode in real time. This is comparable to GSM (Groupe Speciale Mobile) and VCELP (Vehicle version of the Code-Book Excited, Linear Predictive algorithm), the algorithms used in Europe and the U.S., respectively, to compress voice for cellular-phone transmission. Decoding takes 1 MIPS. The algorithm can also be executed on Intel and Motorola microprocessors, but even the floating-point versions require more MIPS horsepower than a DSP IC. Since decoding is less demanding, software playback can be accomplished in real time using most Intel 80386 microprocessors. But encoding with a standard microprocessor, instead of a DSP IC, is another matter. An Intel 80482 DX microprocessor running at 66 MHz would still fall short of real-time encoding, says Mohr.

Music Audio Compression

By now, virtually every engineer in the design community who's vaguely interested in multimedia has heard of the Motion Picture Experts Group (MPEG) of the International Standards Organization (ISO). The MPEG-1 standard, which was finalized early in 1992, describes how a 1.2-Mbit/s bitstream of combined audio and video can be compressed for efficient use of the data bandwidth. The bandwidth would be available either on a CD-ROM or in broadcast applications and then decom-

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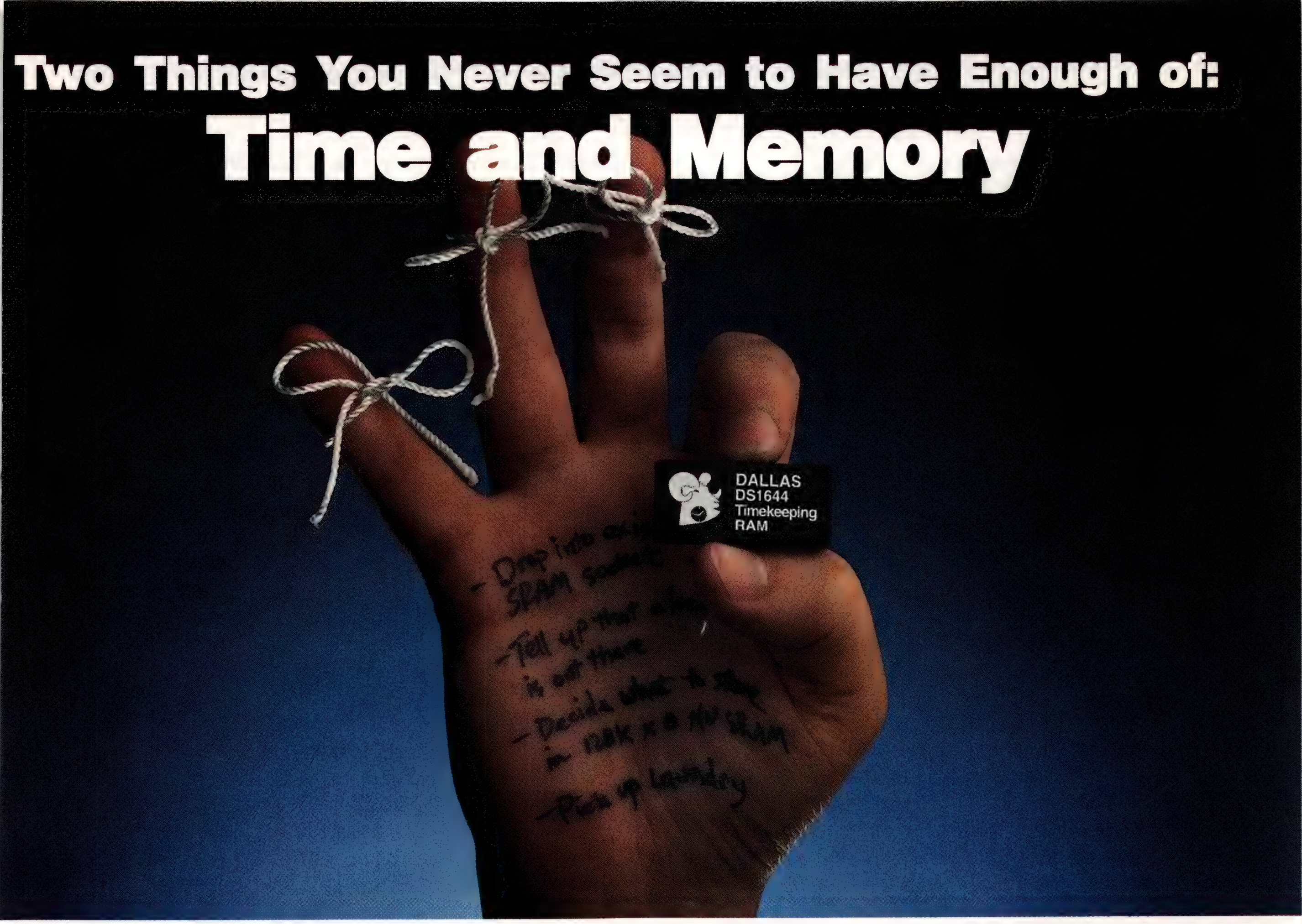

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Because the video and audio components of the MPEG bitstream are processed separately with entirely different algorithms, synchronization is a critical issue. Other important control functions carried in the bitstream are information to manage the coded data buffers to prevent overflow and underflow, information to allow random access startup, and absolute time identification.

MPEG-1 uses time stamps that specify the coding and display time of audio and video as well as the time multiplexed coded data is received at the decoder, all in terms of a 90-kHz system clock. This method provides flexibility in a number of areas, including decoder design, the number of streams, multiplexed-packet lengths, video picture rates, audio sample rates, and coded data rates.

The audio portion of the bitstream supports a bit-rate range of 32 to 256 kbits/s for each of two stereo channels. The 256-kbit/s rate per channel is sufficient to provide CD-quality audio (the option of using 0.5 Mbits for audio, however, leaves precious few bits for coding the video signal). A single-channel 32-kbit/s bit rate is also supported.

MPEG-1's audio-compression coding includes three layers, each providing successively higher performance and with it increased computational complexity. In all three, the time-domain input audio signal is converted into a frequency domain. Also, the first step in compression in all three layers is to bandlimit the signal to 20 kHz, which is the upper limit that the human ear can discern.

In Layers I and II, the algorithm divides the 20-kHz source signal into 32 subbands. These subbands are quantized and coded according to a blockwise, adaptive-bit allocation scheme that's derived from a psychoacoustic model of human hearing. One aspect of the psychoacoustic model is based on the fact that the human ear isn't nearly as sensitive to higher frequencies. When two tones are close to each other in frequency, the higher-frequency, low-amplitude signal is masked by a lower-frequency, high-amplitude tone. This makes it possible to delete the higher frequency, low-amplitude component of the source signal, and by doing so, compress the data stream.

Additional compression is achieved by matching the bit resolution of the signal component to the sensitivity of the human ear. For example, the ear hears 3-kHz frequencies very well, so the 3-kHz component of the data stream is coded at 16-bit resolution. On the other hand, most people can't hear sound at 15 kHz and above, therefore only a few bits are used to code the components in the 15- to 20-kHz band.

Layer II provides more compression than Layer I, which is primarily due to more precise quantization and redundancy techniques. Generally speaking, these are the chips that were introduced to implement MPEG-1 audio-decompression support Layers I and II. This is because Layer III uses a hybrid filter bank to provide more frequency resolution, and that requires additional silicon to implement. Every one of the 32 subbands is further split into higher-resolution frequency lines by a linear transform that operates on 18 subband samples in each subband. The frequency lines are again quantized and coded under the control of a psychoacoustic model. In Layer III, non-uniform quantization, adaptive segmentation, and entropy coding of the quantized values are all employed as a means of achieving better coding efficiency.

Audio decompression using the MPEG algorithm simply involves implementing the inverse filter bank that was used for compression. The MPEG-2 standard is focused on combined audio/video bit rates in the range of 5 to 10 Mbits/s. It accommodates five audio channels, however, instead of just two, and can implement "surround sound" techniques.

Dolby AC-2 Algorithm

MPEG's primary competitor in audio compression are two algorithms developed by Dolby Laboratories Inc., San Francisco, Calif. Dolby's AC-2 algorithm is a two-channel coder that addresses the same product space as MPEG-1. AC-2 codes each channel entirely independent of the other channel. Dolby's AC-3 algorithm, besides being a five-channel coder, differs from AC-2 primarily by taking advantage of redundancies that may exist across channels in multichannel programs, such as a movie soundtrack. As a result, it's capable of higher compression ratios than AC-2.

Conceptually, the AC-2 coders receive PCM audio samples and buffer them into sample blocks. Each block is multiplied by a window function prior to being transformed into a set of frequency-domain transform coefficients. After a block of windowed samples are transformed, the coefficients are grouped into subbands that approximate the critical bands of human hearing. These coefficients are represented in floating-point notation (an exponent and one or more mantissas), with the exponents collectively providing an estimate of the spectral envelope for the audio block.

The next step computes information for a forward-adaptive quantizer that will encode the transform-coefficient mantissas. The information for the quantizer is derived from a dynamic bit-allocation routine that analyzes the subband exponents. The last stage multiplexes the coefficient mantissa bits with the exponent bits, which thus constitutes the data stream for the decoder. The decoder demultiplexes the exponent and mantissa data and basically processes them with inverse transforms.

To implement the algorithm in hardware or software, several other functions are required *(Fig. 3)*. Each analysis interval for AC-2 lasts 10 ms and the encoder has to find the optimal transform block length within each 10 ms to achieve optimal compression (the primary model for determining block

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size is derived from the psychoacoustic model of human hearing.) A block-size controller preprocesses each block on input samples and supplies a block identification number. If the block being analyzed is continuous, or non-changing, then a long block size (512 to 1024 samples) is chosen. If the signals are transitory and higher resolution is needed to represent them, then a relatively short block size of 128 samples is selected.

While the block-size controller is preprocessing the information, a 64-sample delay is introduced in the main audio path. Consequently, the block-size controller can anticipate upcoming events. From this point on, the physical implementation follows the conceptual model just described exactly: data is transformed, quantized, and multiplexed.

According to Dolby Labs, at a sampling rate of 48 kHz, the AC-2 variable-resolution coder using block lengths of 128 or 512 samples provides a subjective quality improvement over a fixed-resolution encoder using either length. Actual hardware implementations offer CD-quality audio performance at 128 kbits/channel, which is a 6:1 compression ratio compared to 16-bit PCM sampled at 48 kHz. Dolby's hardware design specification is based on a Motorola 56001 DSP chip that offers 24-bit precision. The extra six bits prove useful in recovering the two stereo signals. The output of the Dolby subsystem interfaces with 16-bit DACs.

Speech Recognition

Speech recognition is the next frontier in digital audio. Hardware that can understand simple speech, particularly in the case of mobile products, will make even the most elegant graphical user interface (GUI) seem cumbersome.

Speech-recognition algorithms have been around for a long time, and they continue to improve. But over and above the basic theoretical problems of providing accurate processing for continuous speech and speaker-independent inputs, the implementations have generally required workstation-level processing power and massive hard-disk or semiconductor storage.

That situation may soon be resolved by a technology recently patented by Lernout & Hauspie Speech Products, Ieper, Belgium (Lernout & Hauspie's U.S. office is in Woburn, Mass.) The technology combines the highly regarded, phoneme-based Hidden Markov Model (HMM) algorithm with neural network technology. By running HMM on a neural network, the company can implement advanced speaker-independent, continuous-speech on a standard PC platform using a DSP chip as a

coprocessor. Accuracy rates are as high as 96.7%. Storage requirements are roughly 7% of HMM-based products that achieve the same accuracy, but do not leverage neural-network technology.

The basic HMM technology is based on recognition of phonemes instead of words. Typically, languages contain only 40 to 50 phonemes, which are connected together to form enormous word vocabularies. Simplistically speaking, HMM modeling is a probabilistic technique for studying data observations that occur discretely in time.

In a nutshell, the model matches the frequency spectrum of the input to a comprehensive library of human speech sounds. Trying to match a specific sample against a massive library is a daunting task. So the "hidden" part of the model narrows the choices so that the actual frequency-matching aspect of the search is reduced to a relatively small library. The model is termed hidden because the spectrum-matching recognizer is unaware of this part of the algorithm.

After digitizing the sound, the first step is to determine which of the 40 to 50 phonemes in the language are strung together to make the word. Identifying the phonemes reduces the range of the search, and additional limitations are imposed using rules of syntax and grammar. Only after this process is complete does the model launch into brute-force frequency-spectrum matching.

Implementing an HMM model is very compute-intensive and involves spectral-analysis techniques. Such techniques include fast Fourier transforms and frequency-conversion approaches like Cepstrum analysis. For large vocabularies, or to add or change vocabulary words without retraining the speech-recognition system, phoneme-based technology has proven to be faster, more accurate, and less demanding of storage requirements than first-generation word-based systems. The problem has been that while HMM models work well for large words and phrases, system accuracy declines precipitously for short phrases, such as letters or digits. Neural networks provide a good trade-off between accuracy for continuous speech and isolated words.

The memory requirements of HMMs are also drastically reduced by employing neural-network technology. Instead of using one algorithm to crank away at every speech sample to be recognized, the neural network is configured into numerous subnetworks. In typical neural-network fashion, the problem is automatically directed into the network that can handle it most efficiently *(for a complete discussion of neural-network technolo-*

gy, see ELECTRONIC DESIGN, *Feb. 18, p. 51).*

Digital Audio's Future

To date, we've witnessed three fundamental phases for digital audio, according to Satish Gupta, vice president of Media Vision. The first was music synthesis, which began with FM synthesis. It then moved on to wave-table synthesis, and now waveguide synthesis is waiting in the wings.

The second step was the inclusion of speech output, which came in the form of Creative Lab's (located in Singapore) Sound Blaster cards. The first two phases were driven almost entirely by entertainment—games on the PC, says Gupta. The third phase, the ability to record using sampling techniques, introduced a new market: business applications such as voice annotation.

Other aspects of digital audio were also introduced during these first three phases, including text-to-speech and speech recognition. But so far, they have yet to become major parts of the digital-audio equation. The fourth phase, according to Gupta, will include new capabilities. "There will be 'cool stuff' for the audio enthusiast, such as surround sound and reverb," he says. "In other words, the ability to make new sounds. Also, we will see a variety of compression schemes. People are saying that 4:1 is okay, but I have megabytes to store and I need more compression."

Telephony functions will be implemented into the PC on a much broader basis than we have seen so far. "Phase 4 will be characterized by a very dynamic change and a diversity of requirements," he says. Diverse requirements will demand flexibility in the hardware, which in turn can be handled only by digital-signal processing.

"The one thing that has remained relatively constant through all of the phases," he says, "is what the customer is willing to pay for audio capabilities." Today's sound cards with vastly more functionality can be sold for about the same price as early sound cards because more functions have to be squeezed in single chips or chip sets. Gupta believes that the next generation of audio ASICs will integrate a DSP core, plus some of the functions (such as compression and decompression codecs) that provide today's functionality.

The DSP core will primarily handle the Phase-4 functions with a design trade-off between what can be performed in hardware and software. Speech recognition, for example, which is now being done primarily in software, could be handled better by a DSP IC. Over the logh haul, the DSP IC can become an "audio accelerator" analogous to the GUI accelerator in the graphics world, says Gupta.□

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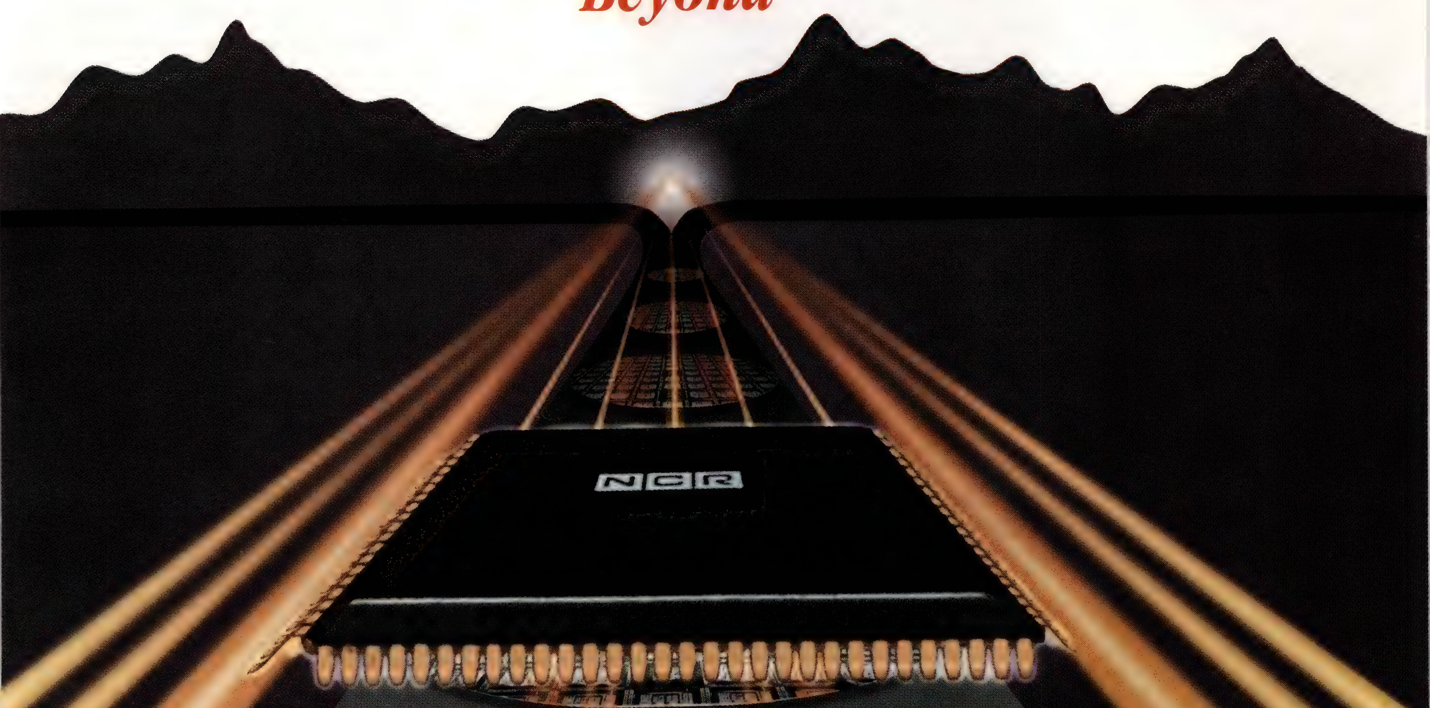

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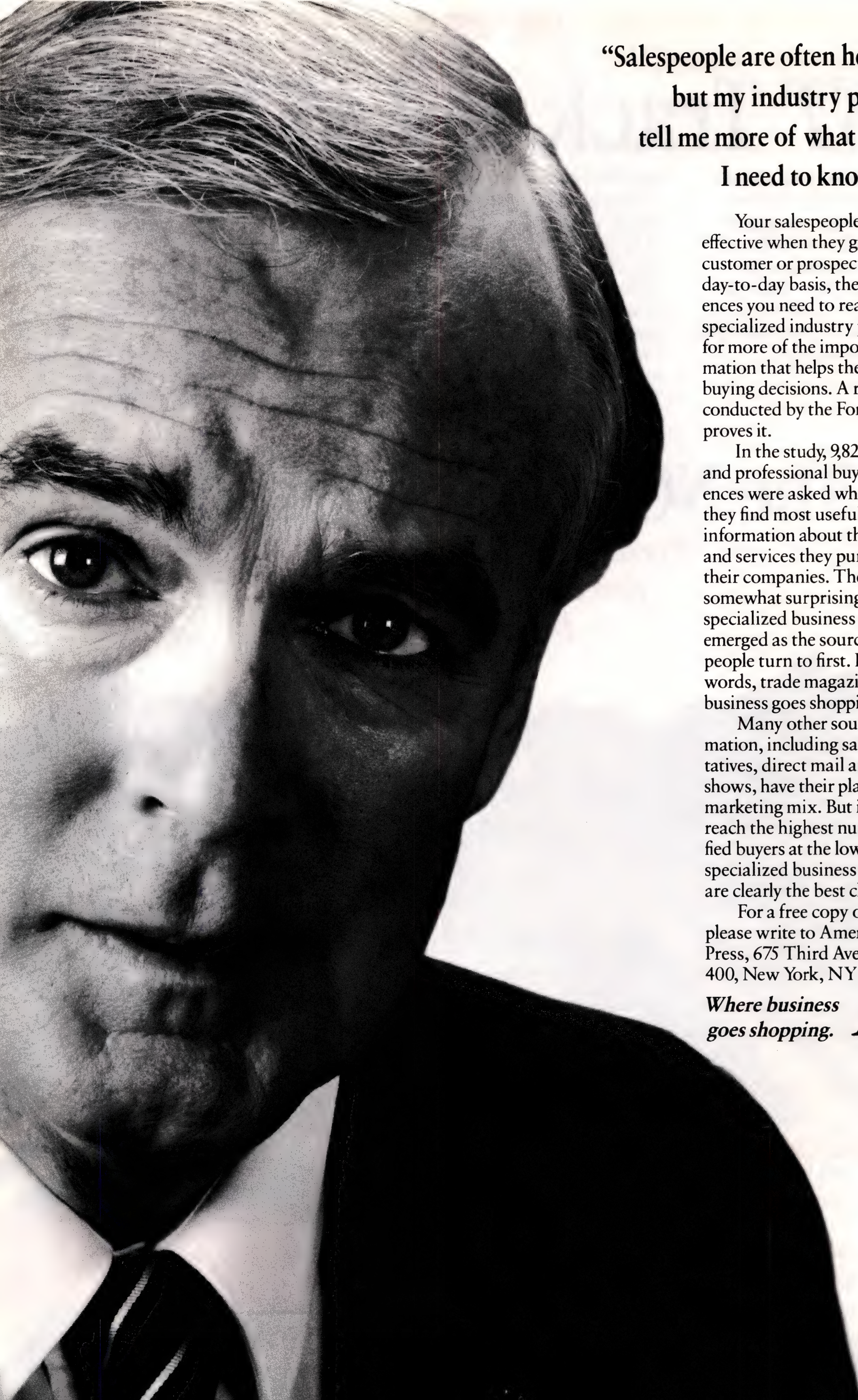

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Connect An FDDI Peripheral To The Sbus

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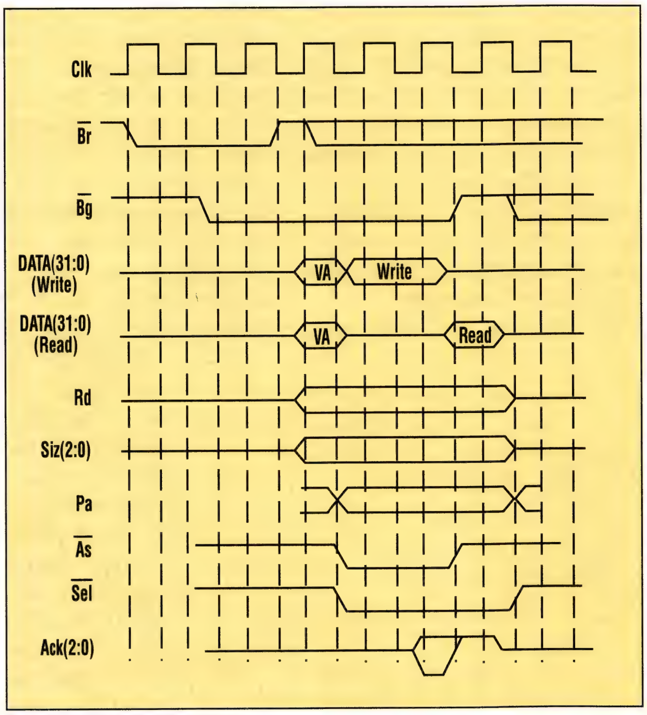
As more and more high-speed peripherals are designed to accommodate the newest standards emerging from committees and working groups, the system designer must find creative ways to connect those peripherals to standard system buses without losing the performance that makes the peripheral attractive in the first place. This article discusses some of the most critical issues involved in interfacing high-speed peripherals to the Sbus system bus, and provides an example of how to interface Sbus to the Fiber Data Distributed Interface (FDDI) standard using only one PAL device as external control (glue) logic.



1. DURING THE basic sbus cycle, the assertion of Bus Request ($\overline{Br}$) signal starts translation cycle. The slave cycle is initiated by asserting both the slave select ($\overline{Sel}$) and address strobe ($\overline{As}$) signals.

Burst buses such as the Sbus have become increasingly common in system use, and involve some creative challenges for the system designer. In general, there are only two characteristics common to every available type of burst bus. First, they are synchronous; that is, the bus transfers are all relative to the bus-clock transitions. Second, the transfer direction cannot change during a burst cycle.

Unfortunately for the designer, the differences between burst buses are numerous. One major differentiator is the manner in which a burst is declared. Some burst buses demand that the master declare the number of bytes for a transfer before the actual burst, while others do not. Another difference involving burst declaration is that some bus definitions have fixed rules for declaring the size of a burst upon beginning each burst, while others are much more flex-

LYNN A. WOODS and AVIEL LIVAY
Motorola Inc., 6501 William Cannon Dr. West, Austin, TX 78735; (512) 891-2214.

ible. Burst termination is also varied between bus types. One standard bus may require a burst to be terminated when a pre-declared burst ends, and others allow the designer to terminate the burst cycle earlier. Clearly, the first interface design decision is which specific type of burst bus the design will interface to.

After the bus type is defined for a given system, the challenges for a designer narrow in focus, but do not become any less significant. In this example, the Sbus system bus is chosen. The Sbus is a popular burst bus designated for use as a chip-level interconnect between components in microprocessor-based systems. It does, however, present a specific set of parameters that a designer must follow, each with peculiarities that can present "gotchas" to the unprepared designer.

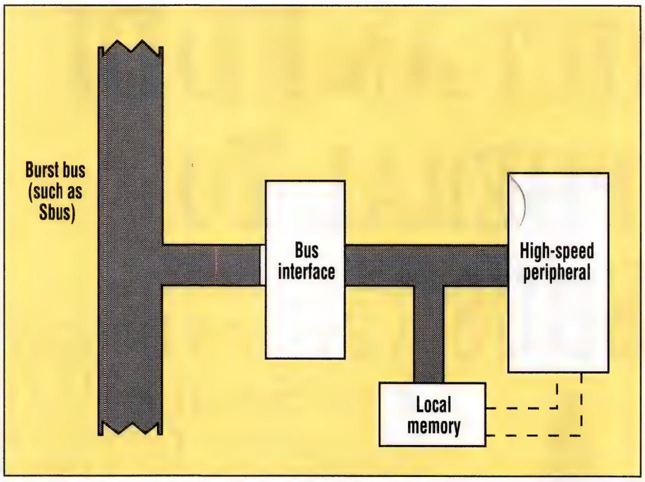
A quick glance at the Sbus definition shows that the Sbus cycle consists of two major portions: a translation cycle and a slave cycle *(Fig. 1)*. The translation cycle results in the physical address being output on the bus. In this part of the Sbus cycle, the control logic must translate between the physical and virtual addresses on the bus. The slave cycle of the Sbus definition results in data being transferred between the master and the slave. Although the slave cycle is relatively simple, it still has some intricacies that can add stress to a design schedule.

In the case of the Sbus, the slave cycle limits the burst to a maximum of 16 word transfers, and the burst size must be pre-defined. Pre-defining a burst size is simple when the system is communicating within its own environment. However, in the case of a communications peripheral that ultimately talks to entities it does not control, it can be difficult to predict an optimal burst size. If a designer chooses a burst size that's too small, it's possible that critical information between the system and the outside world will be lost unless memory is added to the board—an option that adds cost and consumes board space. Conversely, defining a burst size that's too large may cause the system to waste valuable cycle time in terminating a burst that really was too long but was an assured "safe" length. The limitation of the Sbus on the burst size, a maximum of 64 bytes, may require some creative design tactics depending on the page size of the system's memory.

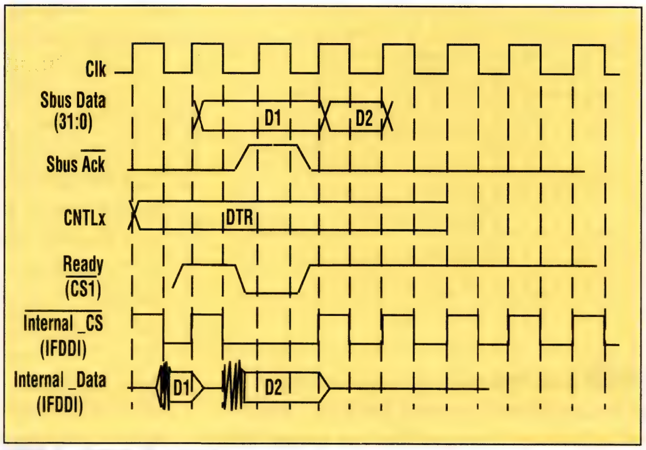
Also, the data-bus definition may present some concerns to a designer, depending on the bus width of the peripheral attached to the Sbus. Some peripherals are designed for 8-bit transfers, while others perform 16- or 32-bit transfers. The Sbus is 32 bits wide with up to 16-word transfers that are a single cycle apiece. If a peripheral has an 8-bit-wide bus, then the Sbus definition is incredibly difficult to meet without a great deal of glue logic or sacrificing data packing in memory. Latches are not too expensive to place on a board, but again, board space is often tight. Because the Sbus uses single-cycle transfers, a design is made much simpler if the peripheral's bus width matches that of the Sbus definition.

According to the Sbus definition, data is presented to the bus master or slave through handshaking between the two entities. When the master writes to the slave, it must keep the data word stable until the slave acknowledges the data. This requires either the external control logic or the peripheral to latch the data, assuring its stability. Conversely, when reading from a slave, the master may sample the data on the clock following the slave's acknowledgement. Select and address strobe signals must remain stable throughout the entire Sbus cycle.

Many designers dread sorting out bus latencies and transfer rates. The maximum bus latency supported by the Sbus protocol is 200 µs. Such a large latency could present problems for high-speed peripherals, especially those involving high-bandwidth communication. In particular, communication protocols using timed token passing allow a particular "station" to transmit data only at specific intervals for a limited period of time. A high bus latency may force a peripheral designed for this type of communication protocol to



2. HERE, THE SBUS SYSTEM is seen with a bus-interface block, which "glues" the high-speed peripheral to the Sbus. There is also a block of local memory included for now, which may be eliminated later in the design cycle if it proves unnecessary for the performance required either by the Sbus or the high-speed peripheral.



3. THE BASIC read cycle from the IFDDI to the Sbus demonstrates the functionality of the IFDDI Ready signal. Note that the PAL device must have a setup time of no more than 15 ns to be Sbus-compliant.

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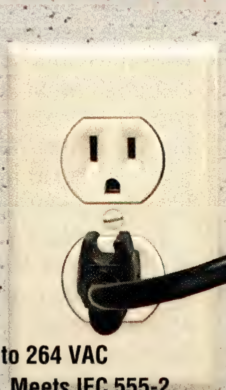

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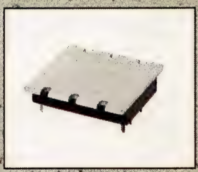

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send out no information for small intervals of time, wasting available bandwidth. This can be avoided only if the system designer plans ahead and prepares to deal with the situation at the start of the design cycle.

Another major area of concern with Sbus implementation is the transfer rate. The Sbus transfer rate depends on the implementation of Sbus, but in general, it uses very high throughput on the order of 40 to 90 Mbytes/s. A high transfer rate combined with a potential high bus latency requires creative planning in the beginning of the design phase.

The last (and perhaps the trickiest) thought-provoking characteristic of Sbus is cycle re-tries. The final decision on how retries are supported must be specific to the implementation, depending on the peripheral that is connected to the Sbus.

At this point in the discussion, a block diagram showing the major components of a system with a high-speed peripheral and Sbus can be sketched out *(Fig. 2)*.

In a typical implementation, the Sbus includes a bus-interface block, which "glues" the high-speed peripheral to the Sbus. Included also is a block of local memory, which may be eliminated later in the design cycle if it isn't needed for the performance required either by Sbus or the high-speed peripheral.

A general discussion of the intricacies of designing for Sbus is important before making critical design decisions, but it typically will not clear up the real issues for a perplexed designer. Narrowing the focus of this design example to a specific type of peripheral should further crystallize the choices that must be made when designing for the Sbus definition.

In this example, the peripheral type chosen is the FDDI communication protocol. FDDI is a timed token-passing ring with a network operating speed of 100 Mbits/s, which is ten times faster than any other approved or completed ANSI standard.

In FDDI, every station repeats what it receives. A station is responsible for transmitting on the ring while it is holding the token.

If the full bandwidth available on the ring is to be exploited, the flow of transmitted data should be continuous. Each station is responsible for stripping off the packets that it transmitted once they have traversed the ring.

As a protocol, FDDI fits well into the concept of burst buses because much of the limitation on the performance of FDDI has come from the system-layer data flows. The Sbus concept of a single address transfer for multiple data transfers streamlines the interface between the upper system layers and the FDDI network, but Sbus was not necessarily defined for peripherals that require such high bandwidths. Even though the two technologies blend well, there is not an exact match.

In connecting FDDI to the Sbus, the first problem to solve is that of bus latency. The FDDI network expects that the data flow will move at a rate of 100 Mbits/s or 12.5 Mbytes/s. The worst-case bus latency of Sbus is 200 µs. This could require up to 2.5 kbytes of memory for temporary storage to be able to perform a continuous transmission on the FDDI network. Where will this memory come from? If the peripheral connecting the Sbus and the FDDI network does not provide memory, then the designer must add memory to a potentially already overcrowded board.

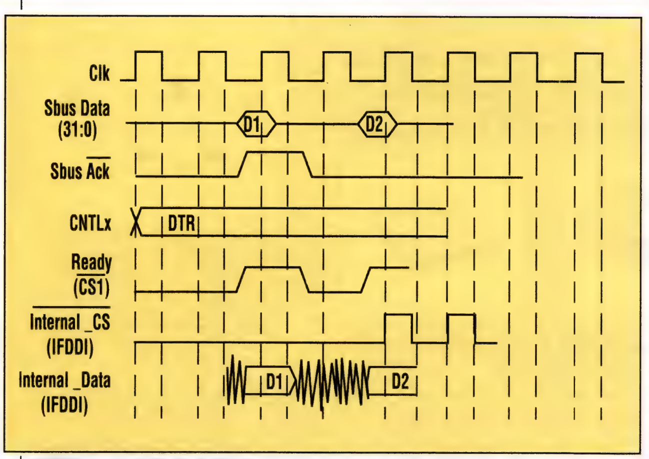
Looking back at the general system diagram *(Fig. 2, again)*, local memory was added at that phase of the design only as a safety measure. It was hoped that the memory would prove unnecessary as the design progressed. Now it's clear that eliminating the memory is possible only if the designer chooses the control logic and the peripheral wisely. A similar issue is that of the Sbus transfer rate. Again, in this case, the solution to this problem is highly dependent upon the particular peripheral attached to the Sbus.

If the peripheral cannot keep up with the transfer rate of the bus, the designer must also deal with cycle retries. Clearly, the designer will have to re-examine these issues once the peripheral and the control logic have been completely defined.

FDDI requires a specific frame structure for the data that the network will be moving. The Sbus is responsible only for transferring data between components in a microprocessor-based system. The designer must provide for both the FDDI protocol as well as the Sbus expectations, and, thankfully, has a number of options available.

In this design example, one may use a peripheral chip that includes a system interface, freeing the designer to be concerned only with the cycle differences between the chip and the Sbus. The silicon takes care of the FDDI protocol-specific structures, and the user is free to worry about the problem at hand. The Motorola MC68840 IFDDI device provides the link between the FDDI network and the Sbus-system environment, leaving the translation between the IFDDI and the Sbus protocol up to the external control logic. The IFDDI assists the designer by providing hooks needed for connecting to the majority of burst buses, while leaving the specifics of each bus protocol up to the designer to implement in their control logic.

Once the major system blocks have been decided upon, the first thing for a designer to be sure of is what the peripheral chip will and will not do to help simplify the design. The MC68840 IFDDI is an integrated



4. THE BASIC write cycle to the IFDDI from the Sbus includes a wait state for the data.

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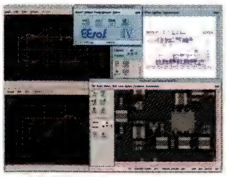

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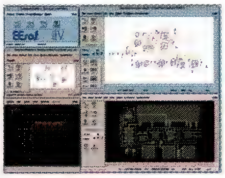

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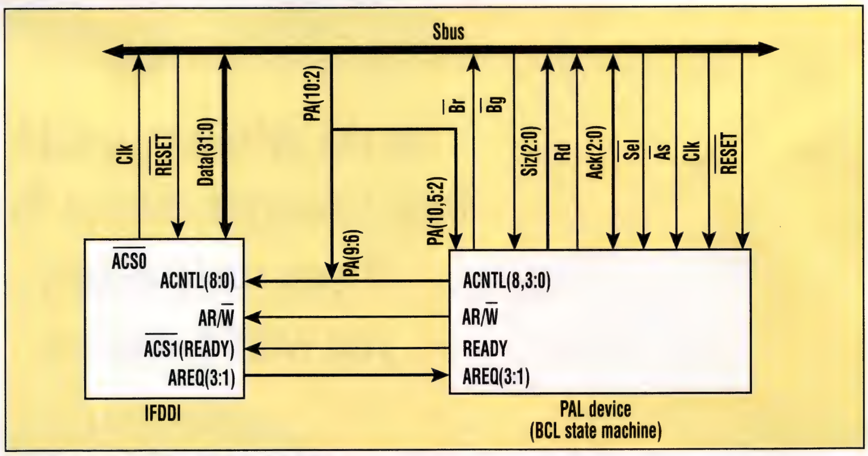
system interface and MAC- and PHY-level device in a 184-pin package. It provides the designer with two 32-bit ports that can be combined into a single 64-bit port, so no external latching is required in connecting the IFDDI to Sbus.

The IFDDI supports a 40-ns cycle time and supplies the designer with up to 8 kbytes of on-chip memory. The on-chip memory allows the IFDDI to support bus latencies in the range of 80 to 300 µs, depending on the configuration and memory allocation defined for a specific implementation. The IFDDI works on a per-cycle access, supporting single-cycle transfers in either big-endian or little-endian modes.

On a slightly more detailed level, the IFDDI is a slave device that is able to become a bus master through arbitration control. It uses a minimal amount of handshaking signals between it and the control logic for cycle translation and interpretation. The IFDDI informs the control logic of the type of cycle it is requesting to have performed through its $\overline{REQ}$x lines. The external control logic uses the CNTLx lines to inform the IFDDI of the type of cycle that it is to perform next. It's actually possible for the control logic to ignore the $\overline{REQ}$x lines for a cycle if a more critical operation is required, as long as the $\overline{REQ}$x lines are serviced on a later cycle. This allows a more simple handshaking scheme between the IFDDI and Sbus through the external control logic.

The most important remaining decisions concern how and when the IFDDI performs a data transfer. This aspect is completely up to the external control logic. The control logic must determine and control the appropriate operation to take place once the IFDDI reaches the burst limit or the data is not valid during a burst. The IFDDI will not force termination of the burst in these cases unless the external logic does so.

The IFDDI also leaves acknowledgment of the state of the data (whether it's good or bad) up to the external control logic. If the external control logic determines that the data contains errors on a given transfer and the error acknowledgement from the control logic is timely, the IFDDI should be able to indicate which address the error occurred on. If the error acknowledgement is late, the external control logic must generate a bus-error interrupt to announce the data-transfer error. By that time, the IFDDI may have already updated the address.



5. A BLOCK DIAGRAM of the Sbus and IFDDI shows all the required signals for proper operation between the IFDDI and Sbus protocols. Such a diagram is helpful as a reference when tracing out the state machine and resulting PAL-device equations.

Because the IFDDI is not an Sbus-specific product, the manner in which certain characteristics unique to Sbus are handled is left up to the designer. The most noticeable of these characteristics is the possibility of cycle re-tries. Retries were added to the Sbus definition because of peripherals that could not keep pace with the Sbus transfer rate. If a peripheral is unable to keep up with the Sbus transfer rate on a specific cycle, the access is repeated, causing a "retry." When using a high-performance peripheral, the retry should not be needed because the peripheral should be able to handle the Sbus transfer rate.

If a designer *must* include the cycle-retry state in a system design for some reason, the best available option is to add external buffers to this design example. In the case of the IFDDI, which is a high-performance peripheral, the external buffers are unnecessary logic and this point is discussed for the sake of completeness only.

The next issue unique to an Sbus application is the transfer rate. The maximum transfer rate supported by the IFDDI in this implementation is 80 Mbytes/s during a master write cycle and 72.7 Mbytes/s during a master read.

Supporting the high transfer rates of this design requires a simple precaution that a designer may overlook until the board is ready for its initial debugging. The IFDDI signals that it is changing the course of an access through its $\overline{REQ3}$ line when one of the following events occurs:

- The direction of the transfer is changed.
- A new buffer with a new address will be read or written.
- No new data is to be read or written.
- The current memory page is changing/incrementing

To keep up with the maximum transfer rates, even when the IFDDI changes the course of a memory access, the IFDDI burst size should be limited to 32 bytes. This assures that the IFDDI won't slow down for a new page operation and will keep pace with the maximum transfer rate. This simple tip will save the designer a significant amount of debug time if preparations are made up front.

Once the global issues in designing for Sbus with the IFDDI are understood, a more intricate discussion of the cycles that the two major system blocks require will simplify the decisions made concerning the external control logic. In this design example, an EP910A Altera PAL device is chosen to control the interface be-

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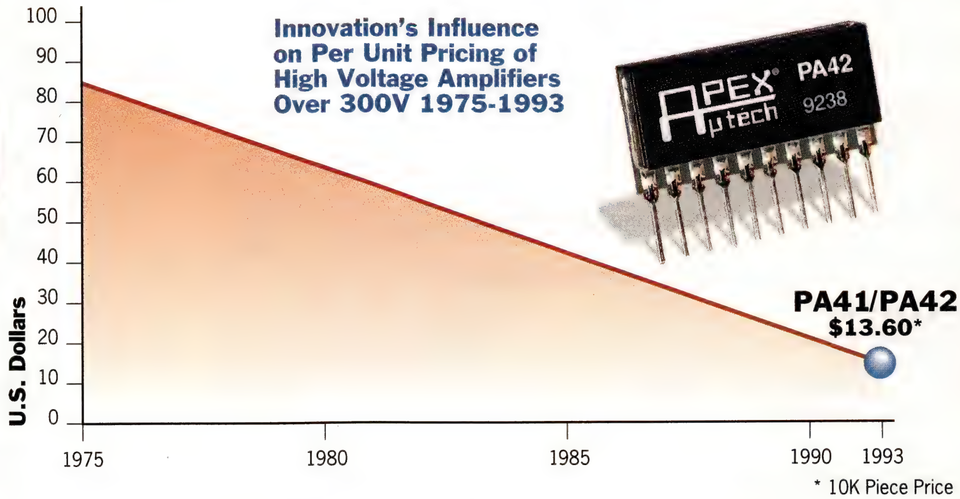

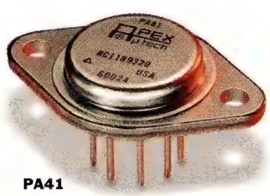

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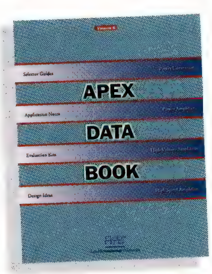

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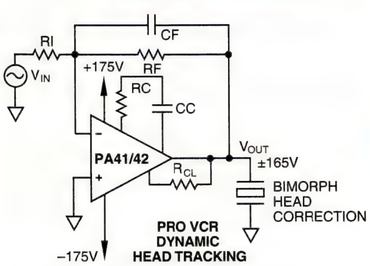

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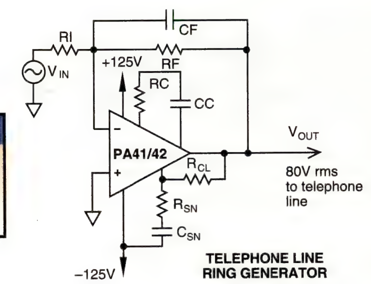

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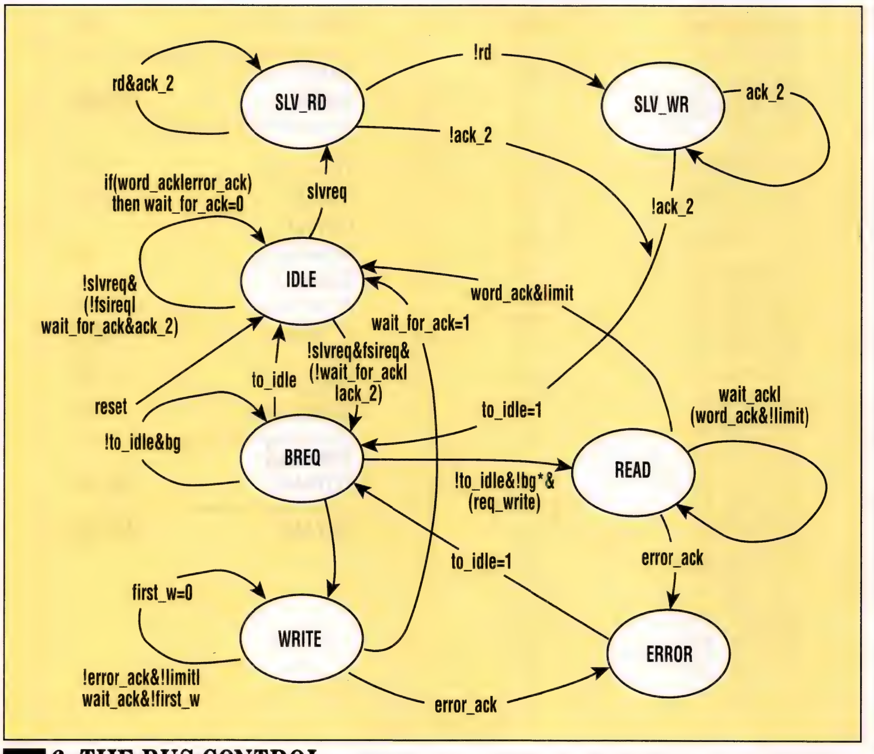

6. THE BUS-CONTROL state machine controls the interface between the Sbus and IFDDI protocols. The accompanying PAL-device equations are tested and available on request.

tween the IFDDI and Sbus.

On the Sbus side, the PAL device must recognize and interpret the translation and slave cycles of the Sbus protocol *(Fig. 1, again)*. The assertion of Bus Request (Br) results in the start of the translation cycle. On the first clock, Bus Grant (Bg) will be asserted for the granted bus master.

The master must sample Bg on the rising edge of the bus clock and then must put a virtual address on the Sbus data lines. The master must also drive the cycle direction (Rd) and the size of the burst (Siz (2:0)) until the end of the slave cycle. The PAL device samples the virtual address on the rising edge of the clock and then translates the virtual address. There's no limit on the translation time for the virtual address. In summary, the master is required to do the following:

- Sample Bg after translating the IFDDI request and asserting the Br accordingly.
- Drive Rd and Siz(2:0) according to the transfer direction and burst size.
- While writing, keep the data word stable until acknowledged by the slave.
- While reading, sample the data on the clock after receiving the slave acknowledgement.

Once the PAL device translates the virtual address, it must begin the slave cycle by asserting both the slave select (Sel) and address strobe (As) and updating the physical address. The bus slave samples As and Sel, and uses the Rd signal to determine the direction of the access. During the cycle, the PAL device must keep track of the acknowledges and the size of the transfer. Upon completion of the transfer, the PAL device must negate As and Bg. One clock following the negation of these two signals, the PAL device must negate Sel.

Note that before beginning a new cycle, Bg should remain negated for at least one clock cycle.

There are essentially four requirements that the PAL device must meet to successfully connect to the Sbus and implement the required state machine. First, the PAL device must have a setup time of no more than 15 ns to be Sbus-compliant. Second, the PAL device implements an Sbus master by fulfilling the following requirements:

- Interpreting *from* Sbus : RESET, Clk, Bg, and Ack(2:0).
- Generating *to* Sbus: Br, Siz(2:0), Rd and their respective output enables.

The third requirement is that the PAL device must implement a compliant Sbus slave by fulfilling the following requirements:

- Interpreting *from* the Sbus: RESET, Clk, As, Sel, and Pa(10,5:2).
- Generating Ack2 and the data output enable *to* the Sbus.

The fourth and final task the PAL-device state machine must perform is controlling the IFDDI by interpreting the AREQ(3:1) signals and generating ACNTL(8,3:0), AR/W, and READY. The exact timing that the state machine must implement between the IFDDI and Sbus can be shown in two timing diagrams *(Figs. 3 and 4)*.

After examining the major blocks and required handshaking signals, the generic block diagram of Figure 2 should be replaced with a detailed diagram of the entire system. Such a diagram may not be as detailed as a schematic, but is helpful as a reference when tracing out the state machine and resulting PAL-device equations *(Fig. 5)*.

The bus-control (BCL) state machine implemented in the PAL device is the most critical piece of a design when using the IFDDI to connect to the Sbus. Upon every rising edge of the clock, the PAL device will sample the new state of the inputs. The new state of the machine and the outputs of the PAL device depend on the previous state of the state machine and the current inputs to the PAL. The first, and most basic, state is the IDLE state *(Fig. 6)*.

In this state, the IFDDI REQx lines are idle and the Sbus is not requesting any operation. From the IDLE state, the BCL is able to move either to the master cycle or a slave access. The IFDDI will toggle its REQx lines when it requires a read or write cycle. This will move the state machine into the BREQ state, which will assert Br and result in the

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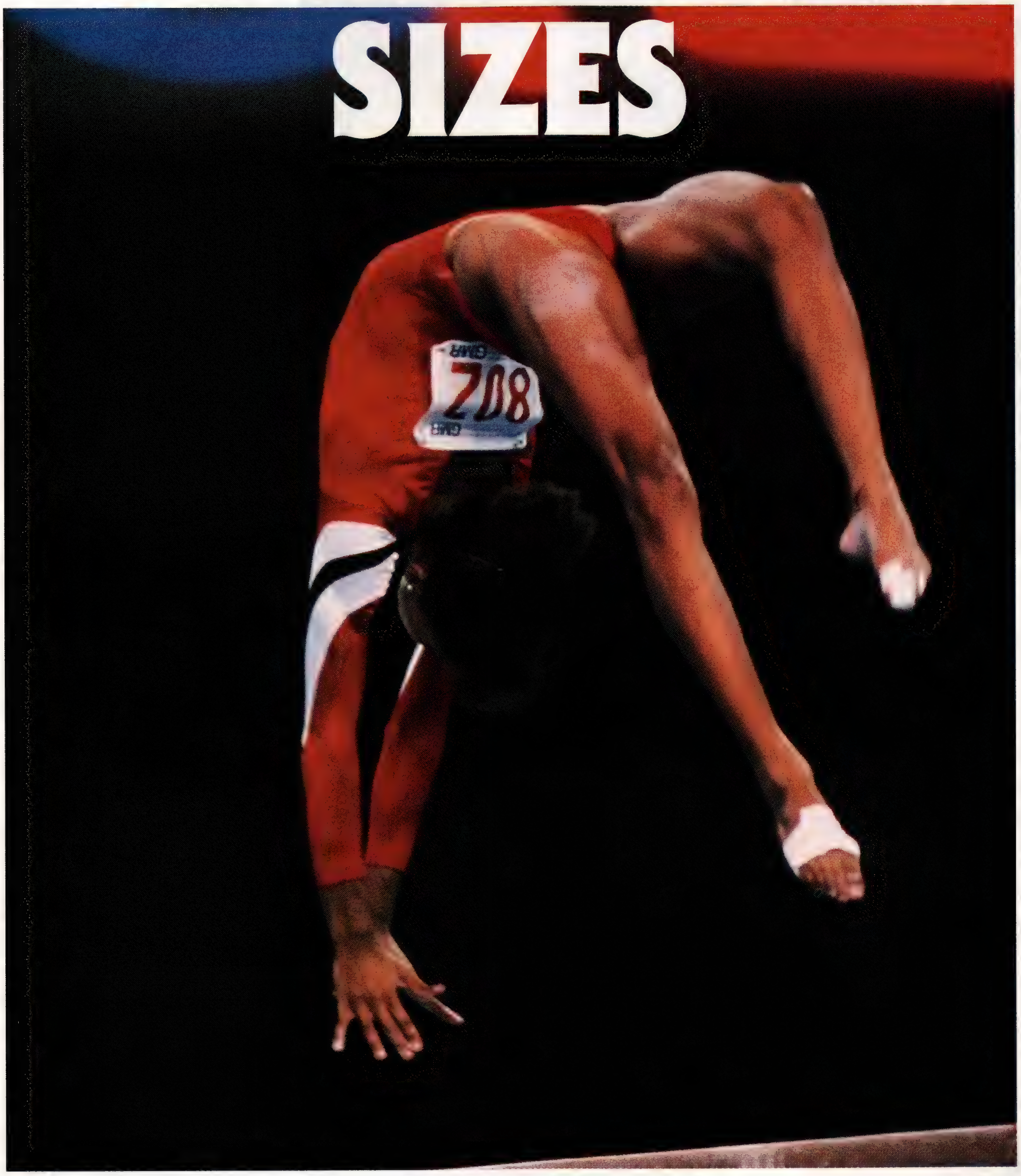

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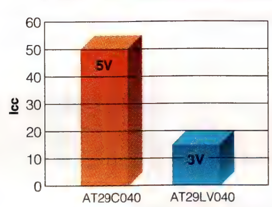

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burst address being read. When a bus request is granted, the state machine moves either to the READ or WRITE state. If the IFDDI is requesting that it be read by the Sbus, a master write cycle is performed. In the converse situation, a master read cycle is performed. Both the master read and write cycles transition back to the IDLE state in a non-error condition. If an error acknowledgement occurs, the state machine first transitions to the ERROR state, after which it returns to the IDLE state.

When the Sbus requests a slave access, the state machine will move to the SLAVE_RD state. If the slave access requested is a slave read, READY is asserted at the end of the cycle and the slave access is finished. The end of the slave access results in the state machine moving back to the BREQ and, finally, to the IDLE state. If a SLAVE_WR is requested, the state machine transitions to the SLAVE_WR state, and then back to the IDLE state.

This brief discussion of the requirements and some of the "gotchas" in designing a system with a high speed peripheral and Sbus is able to cover only a snapshot of the most critical issues.

This example demonstrates that interfacing to the Sbus protocol requires only fine tuning of a state machine when taking advantage of the flexibility of the IFDDI and a PAL. After examining the best solutions to the most critical issues, a designer should now be able to adjust this snapshot for the specific requirements of their design.

Lynn Woods, an applications engineer for the data communications group at Motorola, received a BSEE from Virginia Polytechnic Institute and State University, Blacksburg.

Aviel Livay, a design engineer for the MC68840, holds a BS in computer engineering from Technion - Israel Institute of Technology, Haifa, Israel.

HOW VALUABLE?	**CIRCLE**
HIGHLY	511
MODERATELY	512
SLIGHTLY	513

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Field sales and service management applications will propel the U. S. market for wireless computing applications to hit nearly $10 billion by 1997, according to a report by Venture Development Corp. The Natick, Mass., company's report, *The U. S. Market for Portable Computing and Wireless Communications in Field Sales and Field Service*, predicts that the thriving market will grow at least 40% a year over the next five years.

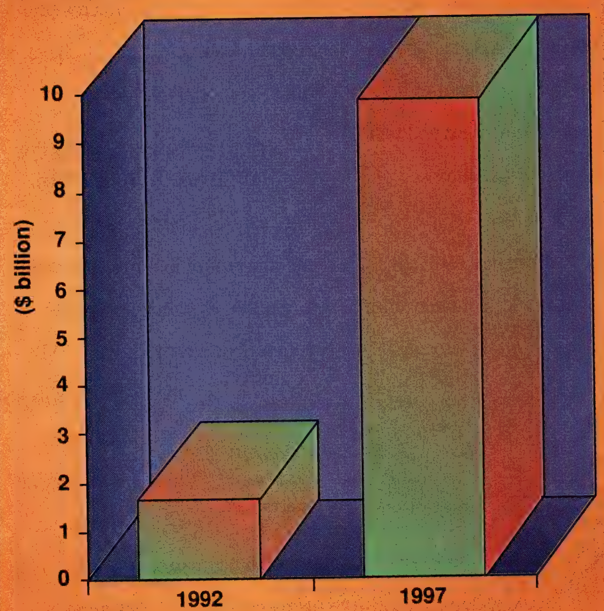
As in many other electronic products, the cost for notebook computers is dropping even as technical improvements are supplying cost-effective wireless data communications. Portable computing hardware will grow at 43% a year through 1997 while the smallest segment, that for RF/cellular modems, is projected to expand at 77% a year.

Portable computing/wireless field applications are expected to make inroads in fields as varied as retail and wholesale, medical and health care, insurance, data processing, real estate, and finance.

On the hardware side, the market for personal digital assistants (PDAs) is ramping up, though not as explosively as some analysts had predicted earlier this year. About 65,000 units should ship in 1993, according to BIS Strategic Decisions.

The Norwell, Mass., market research company also forecasts that communicating PDAs will be key as the wireless network infrastructure expands. The recent agreements between Time-Warner and U. S. West and AT&T and Viacom, among others, are evidence of the convergence of voice and data, the researchers say.

PORTABLE PRODUCTS WILL HANDLE FIELD, SERVICE APPLICATIONS



Source: Venture Development Corp.

YOUR CAREER

Do you want more satisfaction from your job? Do you want to be more productive at work? To help accomplish both goals, form alliances with the engineers who have the same boss you do. That's what employees at major organizations throughout the country are being taught in a new training process called Peer Coaching. The process, created by Blessing/White Inc., of Princeton, N. J. recognizes that engineers need to leverage their peers to survive because peers are a bigger and more reliable resource than the boss is. The process brings across this advice:

Meet regularly with your peers to share new ideas, best practices, insights about the suppliers and customers you have in common, and solutions to common problems. It's rare to encounter a problem someone else hasn't handled successfully before.

- If you're confused by your supervisor's words or behavior, ask peers who know him better.
- When you have to criticize the boss, ask the peer who has the best relationship with her to do it.
- Work together with peers on tasks each of you handle such as creating budgets, forecasting personnel needs, creating cost-reduction plans, and so forth.
- Before meeting with the boss to get approval for a decision, proposal or budget request, get advice from your peers and rehearse your presentation with them. Let your peers toot your horn for you. It's much louder that way. And be ready to return the favor, of course.
- Confide only in peers you trust, of course. Ask that your discussion be kept confidential. When the topic is really sensitive, confide in a friend rather than a peer.

Note that competition can prevent cooperation. Usually the benefits of cooperating outweigh the risks. Peers should give each other permission to say no to working together on occasion.

QUICK REVIEWS

Not a developer's manual, *Inside Windows NT* by Helen Custer describes how Microsoft's operating system was developed—from its inception in 1988 until its final snapshot last year. Project leader Dave Cutler had spent 17 years at Digital Equipment Corp. developing operating systems and compilers, including the VAX/VMS OS. Some of the development team's goals were to incorporate in the new OS Posix compliance, security, extensibility, portability, reliability, and robustness. Custer gives an NT system overview and goes on to discuss NT's object manager and object security, processes and threads, Windows and protected subsystems, the virtual memory manager, the kernel, the I/O system, and networking. Published by Microsoft Press, the 385-page book lists for $24.95; (800) 677-7377; fax (206) 936-7329. (ISBN 1-55615-481-X). CIRCLE 460

OFFERS YOU CAN'T REFUSE

View and manipulate timing diagrams on your PC with the Intel486 Interactive Databook from Chronology Corp. The package combines a databook and a 3.5-in. disk that contains 99 timing diagrams for various versions of the Intel 80486 processor. Also included are 19 electronically readable timing libraries.

The disk has a special read-only version of TimingViewer, the company's interactive timing-analysis software that lets users view and experiment with the timing diagrams and library data. Also, the libraries are supplied in ASCII format so they can be used with most spreadsheet software. The Intel486 Interactive Databook costs $49.

For more information, contact Chronology Corp., 17411 N. E. Union Hill Rd., No. 100, Redmond, WA 98052; (206) 869-4227.

—LISA MALINIAK CIRCLE 461

A free *Guide to Public Online Services* lists bulletin board systems (BBS) as diverse as the users who access them. Among the companies listing their customer support BBS are Logitech, Gateway 2000, Lynn-Western New Service, AST, Accolade, ALR, Dell Computers, and Micrografx. Other bulletin boards cover travel, 12-step recovery, the environment, online shopping, and many other topics. The guide is available from Galacticomm Inc., 4101 SW 47th Ave., Suite 101, Fort Lauderdale, FL 3314; (305) 583-5990; fax -7846; BBS -7808. CIRCLE 462

A sample—two issues—of Patricia Seybold Group's monthly report *Open Information Systems* is free upon request. The report covers open, distributed systems, database management, downsizing, and integration options, among other issues. The report goes for $495 a year for 12 issues. For more information, contact the Patricia Seybold Group, 148 State St., 7th Fl., Boston, MA 02109; (800) 826-2424 or (617) 742-5200; fax -1028. CIRCLE 463

An applications portability guide from NIST covers standards for different functions and services that must work together—from the human interface with the computer to applications and interconnections with networks. NIST SP 500-210 is $6.50 from the Superintendent of Documents, P.O. Box 371954, Pittsburgh, PA 15250-7954 (stock no. 003-003-03222-1).

HOT PC PRODUCTS

A new edition of analysis and diagnostic software, WindSleuth Gold Plus helps users install, configure, and troubleshoot hardware and software running under Windows. The $189 program simplifies installing multimedia boards, CD-ROM drives, fax/modems, scanners, networking, and other adapters with libraries of data files that supply accurate DMA, IRQ, and port requirements for specific devices.

Contact Dariana Software, 5241 Lincoln Ave., Suite B5, Cypress, CA 90630; (800) 892-9950; (714) 236-1380.

CIRCLE 465

A document manager, Golden Retriever from Above Software helps users create, store, organize, track, and search for documents and files. Users can name files with up to 256 characters. Golden Retriever also organizes files generated by Windows and DOS applications into file drawers and file folders by project or subject, much like a paper document, rather than by directory, subdirectory, and application. The program carries a list price of $99.

Contact Above Software, 2698 White Rd., Suite 200, Irvine, CA 92714; (800) 344-0116; (714) 851-2283.

CIRCLE 466

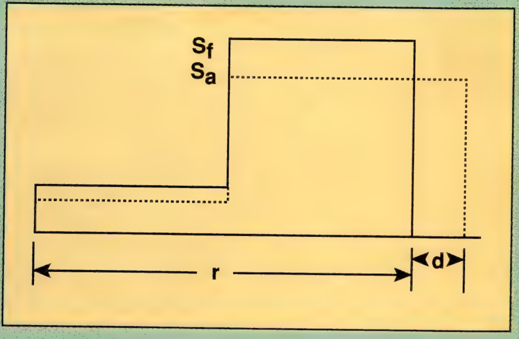
KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (408) 446-4458; fax (408) 253-6085

The illustration in the last column supplied a graphic link between the development staffing profile and the profits returned by the product from the market. This column adds a new concept, the staffing ratio, to aid further exploration of the relationships between staffing, timing, and profits.

The staffing ratio is defined as: Staffing ratio $= S = S_a/S_f$, where S_a = the actual staff working on the project; S_f = the full staff needed to complete the project in time "r." To apply the staffing ratio concept, recall the speed profile from previous discussions.



Speed profile definition phase staffing runs at 20% of S_f and at 100% of S_f during the execution phase. This profile gets the product's development work accomplished in the amount of time equal to "r." Nonetheless, a common occurrence in industry is to actually staff S_a at a level that is somewhat below the full staff number. When this is done, the area is preserved but the project is delayed by the time "d" that is shown in the illustration. The expression to compute d is:

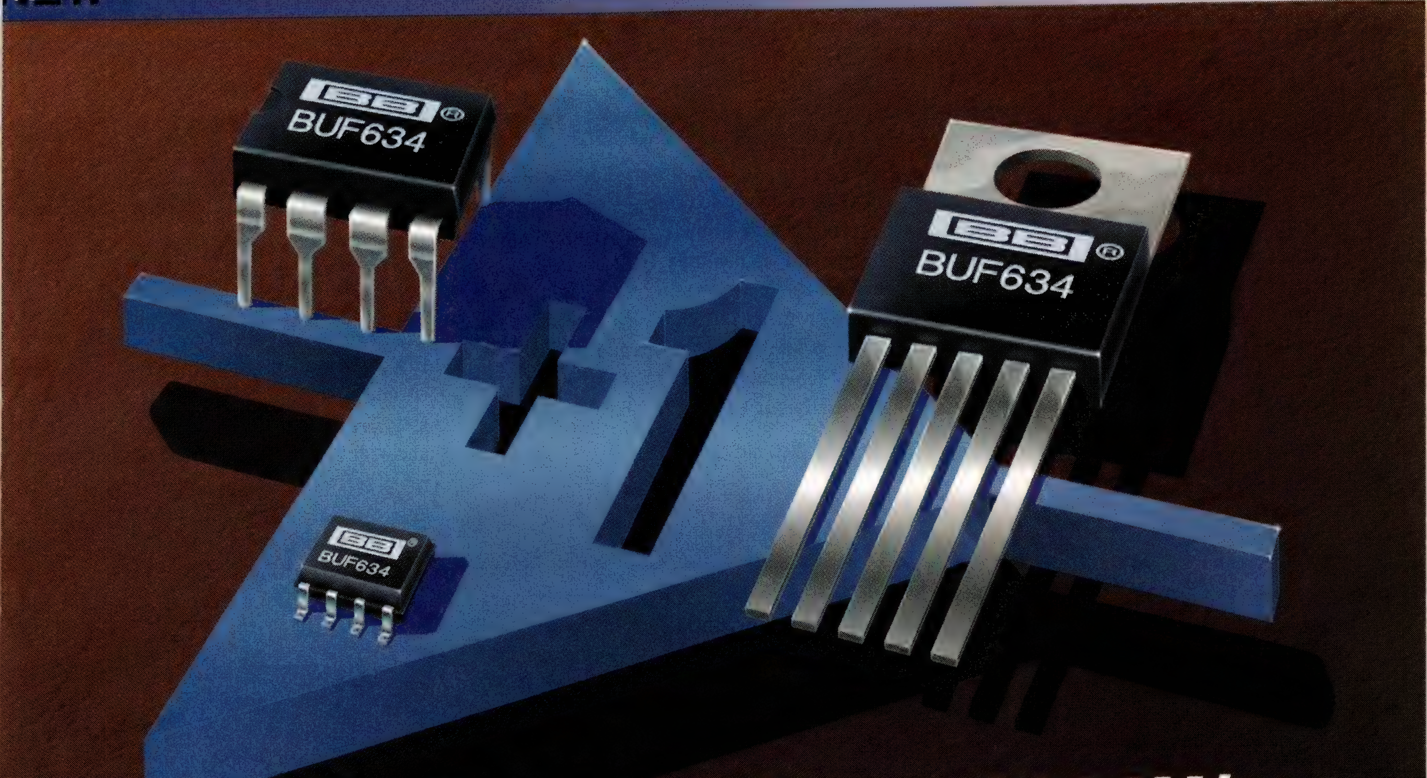
$$d = r(1 - S)/S$$

As a result, a project executed at full definition and execution phase staff, S = 1, completes with a delay equal to zero. A project run at one-half staff, S = 0.5, completes with d = r or a total development time of 2r.

This simple relationship between staff level and delay can now be linked to the equations for cost of lateness developed in previous columns. I'll pick up on a primary link in the next installment.

More information on this topic is contained in New Product Development: Design and Analysis, which can be obtained by calling Time to Market Associates.

NEW



250mA Buffer Amp Slews 2000V/µs

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BUF634 is a high speed, unity-gain buffer amplifier that delivers 250mA output and 2000V/µs slew rate—all in a tiny SO-8 package. Its low price, high performance, and ease of use make BUF634 ideal for a wide range of applications. It's an excellent driver for valves, solenoids, video, and even headphones.

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BUF634 can be used inside the feedback loop of op amps to increase output current, eliminate thermal feedback, and improve capacitive load drive. Its bandwidth can be pin-programmed for 30MHz with 1.5mA quiescent current or boosted to 180MHz with 15mA quiescent current. BUF634 is the simple solution for all your buffer needs.

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- Output current..250mA
- Slew rate...2000V/µs
- Pin-selected bandwidth ....30MHz to 180MHz
- Quiescent current ....1.5mA (30MHz BW)
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CIRCLE 160 FOR U.S. RESPONSE CIRCLE 161 FOR RESPONSE OUTSIDE THE U.S.

DID YOU KNOW?

... that sales of personal computer application software in the U. S. and Canada amounted to $1.6 billion in the second quarter of this year, a nearly 14% increase compared with the second quarter of 1992. Sales of Windows applications increased 53% in the quarter, accounting for 48% of industry revenues. Meanwhile, sales of DOS applications declined 16.2% for the quarter while Macintosh applications increased 14%. Word processing is the largest category among applications, followed by spreadsheets and database programs. Sales of Windows databases continue strong while Macintosh database sales were up 90% for the quarter and DOS database sales declined 26%. The fastest growing category is home education, where sales have been strong for three quarters. Sales were up 55% in the quarter, amounting to nearly $36 million.

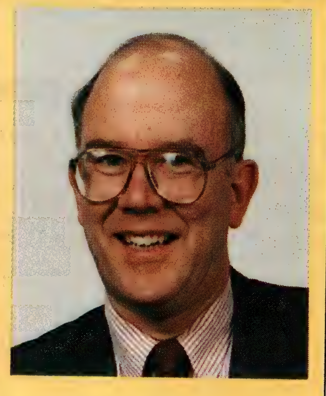
The Software Publishers Association, Washington, DC, (202) 452-1600.

TALES FROM A SKUNK WORKS

We've been discussing contrasts in management style and barriers to skunk works. The poor results from generic downsizing are proven and the dark ages should be ending. We can expect a shift from slash and burn management—but to what?

Business "re-engineering" is popular. Most embrace it as another form of process and cost cutting, but it can also create empowered teams and drive organizational change. I've always viewed consulting assignments as opportunities to serve as an organizational architect for new product and new business teams. Re-engineering makes such teams, and skunk works, better understood by top management—and perhaps more socially acceptable.

You can use this trend to drive change, but it will not be easy. Consider what would result in most companies if the CEO walked into a mid-level manager's office one day, and said, "That fellow Trudel is right! Go run that skunk works that you've wanted to."



In most cases, the likely result would be unmitigated catastrophe. Failure would mark the end of empowerment and skunk works at that company for a long time. They would relapse to industrial age process and micromanagement. Empowerment without training, coaching, and practice is a formula for disaster. Few would consider putting tennis rackets into the hands of beginners and sending them to Wimbleton. No one would consider putting novices into the left seats on airliners and turning them loose. In business, tragically, we often do the equivalent.

I have *never* seen a time when investment in training is so low. Half of the industry invests less than 1% of its budgets on enhancing skills in the workforce; three quarters of the companies spend less than 2% on developing essential skills.

I gave a lecture at an electronics expo and overheard a breakfast discussion. The silver-tongued senior salesman was breaking in the smart young assistant. They worked for a successful venture-capital backed firm that did CAE software.

"If you spend an hour training four engineers, that is half an engineering day wasted. Customers can't afford that." The words chilled me. Who can learn even a new word processor in an hour?

Under the slash-and-burn approach, employees worked cheap and obeyed orders. Successful skunk works require vastly different behavior. Even getting started requires shared models, training, and a lack of fear. Developing these things takes shelter, time, and coaching. Learning from experience is much too slow and uncertain for today's world. When they give you a shot at change, empowerment, and skunk works, bring in an expert to serve as a change agent, mentor, and guide. Now 52% of firms *regularly* obtain help from outside consultants for new product development. The right consultant can be the best investment you've ever made.

John D. Trudel lectures and provides business development consulting. Trudel is founder and director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 690-3300; fax (503) 543-6361; e-mail address: JohnTrudel@aol.com. He is the author of High Tech with Low Risk. *To order, phone (503) 280-8547.*

QUICK NEWS: CONFERENCES & SEMINARS

Software Engineering '93 and its applications will be held in Paris Nov. 15–19, 1993. Sponsored by CIGREF (French companies group for information technologies), the SEE (French electric and electronics engineers society), and Syntec Services Informatiques and organized by EC2, the conference aims to cover software engineering development and applications such as data processing, industrial computing, and embedded and real-time systems. Contact EC-2, 269-287 rue de la Garenne, 92024 Nanterre Cedex, France; +33.1 47 80 70 00; fax -66 29. CIRCLE 467

Concurrent product development, also called concurrent engineering, is key to improving product quality while lowering costs. The Concurrency Group management consulting firm offers assessments, implementation workshops, and methods for improving a company's product-development process. Consultations account for such factors as the ability to accept change, competitive product positioning, and explicitness of goals. For more information, call the Concurrency Group, 51 Sawyer Rd., Suite 150, Waltham, MA 02154; (617) 642-8785. CIRCLE 468

The 4th International Conference on Applications of Software Measurement (ASM '93) will be held Nov. 7–11, 1993 in Orlando, Fla. Tutorial sessions include software measurement: an engineering process, managing with metrics, measurement as a software management tool, and metrics plan development. Contact ASM '93 registrar, 3000-2 Hartley Rd., Jacksonville, FL 32257; (800) 423-8378; (904) 268-8639; fax -0733. CIRCLE 469

The 1993 Technology Summit will be held Nov. 4–5, 1993 at the Marriott Hotel, Santa Clara, Calif. The summit, modeled after the economic summit, is sponsored by the UC Berkeley Roundtable on the International Economy (BRIE) and UC Berkeley Extension. Government representatives scheduled include Thomas Kalil, director for science & technology, National Economic Council; and Lionel "Skip" Johns, Office of Science and Technology Policy, among others. For program information, contact Harvey Stern, UC Berkeley Extension Southbay, 800 El Camino Real, Suite 150, Menlo Park, CA 94025; (415) 323-8141; fax -1438; e-mail southbay@garnet-.berkeley.edu. CIRCLE 470

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CIRCLE 521

SIMPLE RS232 SYNC TO ASYNC CONVERTER

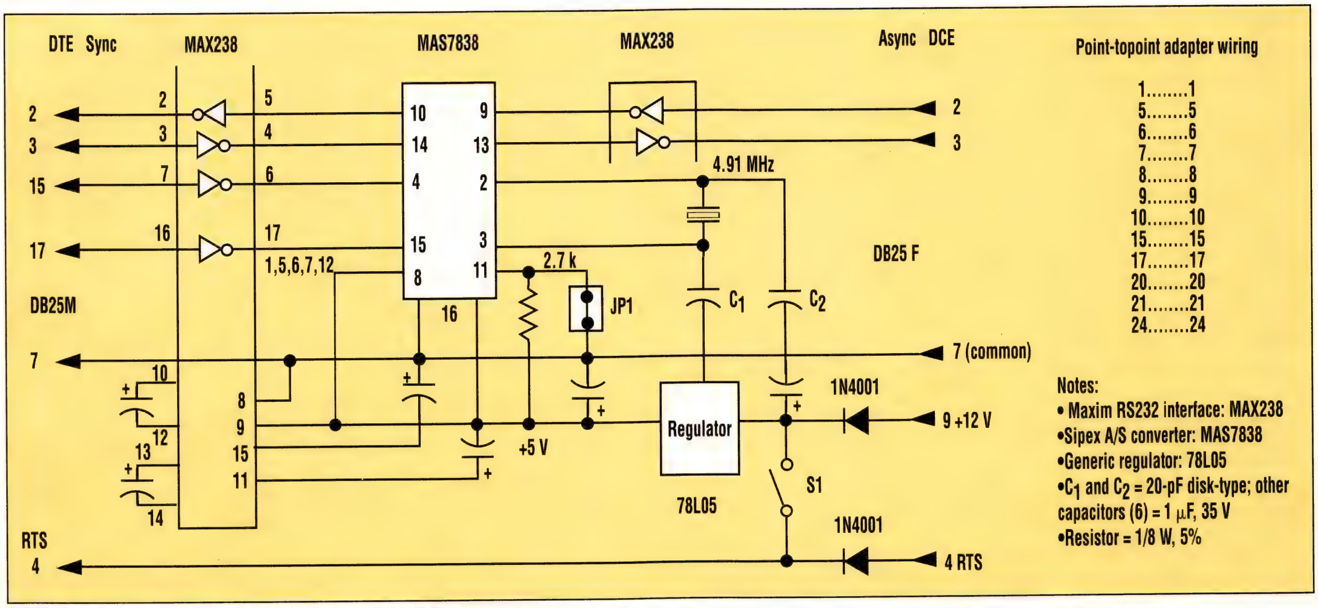
CHARLES HARTLEY
P.O. Box 614, San Carlos, CA 94070.

The surge in popularity for synchronized data communication can be traced, in part, to the onslaught of new "wireless" network extension devices. In the past, an asynchronous speed of 4800 baud was considered fast. Thus, a 19.2-kbit synchronized communication device could handle async data up to 4800 baud by oversampling without experiencing many problems.

But, with today's higher asynchronous rates and the requirement to operate at equal data speeds, oversampling is no longer adequate to link two systems.

This simple converter *(see the figure)* consists of two ICs and a voltage regulator. The Sipex MAS7838, which acts as the converter, selects the conversion speed to that of the synchronized data clock. It has internal switches and registers to perform the async to sync, or sync to async, conversion. The Maxim MAX238 provides the RS232 drivers and receivers for interfacing with the data bus. These chips require a 5-V dc power supply; a generic 78L05 reduces the +12 V at the DB25 pin 9 to the +5 V needed. A crystal frequency of 4.91 MHz is suitable for converting to 19.2 kbits or a sub-multiple (9.6, 4.8, 2.4, etc.). Two 1N4001 diodes protect the external RTS (ready to send) control circuitry if the RTS is enabled by S1. When JP1 is removed, the converter is transparent in the sync mode and no conversion will take place.

The completed unit is mounted atop a universal breakout adapter, and the control lines are jumpered according the chart in the figure. The physical size is approximately 1 by 2.25 by 2.5 in. and will easily plug into the DB25 socket on a synchronized data communications equipment (DCE) communication device.□



THIS SIMPLE SYNC TO ASYNC converter overcomes the inadequacy of oversampling when dealing with high async rates.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award.

Send in Your Ideas for Design
Address your Ideas-for-Design submissions to Richard Nass, Ideas-for-Design Editor, Electronic Design, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

CIRCLE 522

12-BIT DAS PROVIDES 2500-V ISOLATION

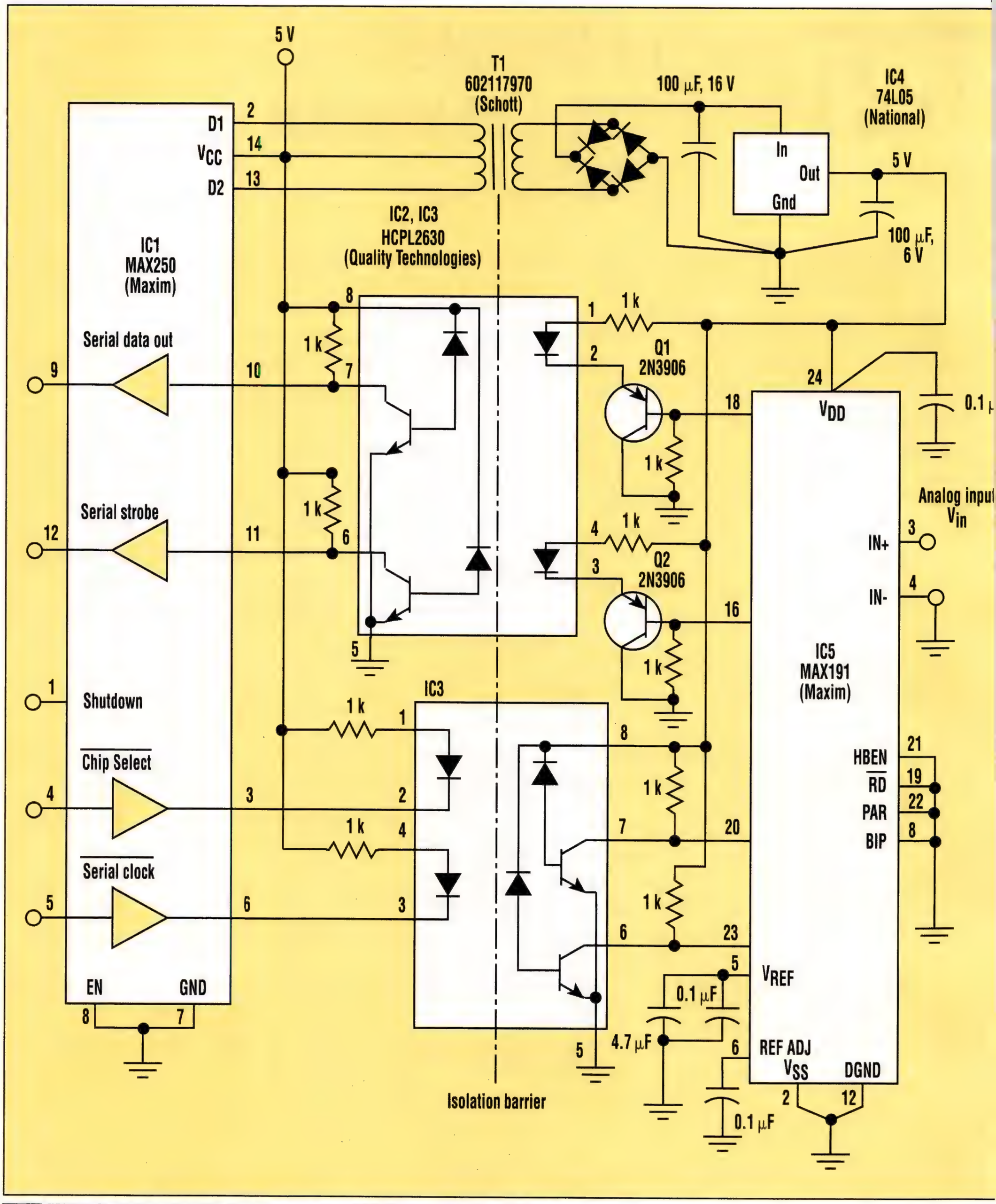
DANA DAVIS
Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA 94086; (408) 737-7600.

A remote data-acquisition system (DAS) requires some form of isolation if it must accommodate large ground-potential differences. One solution is to isolate the analog signal from the rest of the circuit, but that approach can be tedious.

A more practical scheme, which includes a sample-and-hold amplifier on the analog-to-digital converter (ADC), isolates only the converter's

I/O lines *(see the figure)*. The resulting isolation barrier can withstand as much as 2500 V dc for one minute. Basically, the isolation barrier consists of two high-speed optocouplers (IC4 and IC5) and a transformer that conveys square-wave power from IC1, across the isolation barrier, where it powers the rest of the circuit. Obviously, the converter's serial-data outputs reduce the number of optocouplers required.

In the operation of the circuit, IC1 generates out-of-phase square waves, at D1 and D2, which are rectified, filtered, and regulated to 5 V. The chip also includes two data drivers and two data receivers (compatible with SPI and Microwire serial-interface standards) that communicate with the microprocessor. The 12-bit sampling analog-to-digital converter (IC2) offers 5-V operation, a 0-to-5-V input range, and an on-board voltage reference. Transistors Q1 and Q2 boost current drive to the optocouplers.□



THIS REMOTE DATA-ACQUISITION SYSTEM only isolates the ADC's I/O's lines. As a result, the isolation barrier can withstand as much as 2500 V dc for one minute. The circuit includes a 12-bit, 25-µs ADC, 2500-V isolation, and a serial-data interface.

CIRCLE 523

Manually Control Heater Output

EINAR ABELL
ADA Instruments, 41899 South Fork Dr., Three Rivers, CA 93271; (209) 561-0618.

Built around an LM339 quad comparator, this circuit provides manual control of the output of a resistive heater or other load with a long time constant. The circuit's design uses minimum parts, thus its low cost, and generates very low RFI.

In the circuit *(see the figure)*, it can be seen that comparators a, b, and c form a low-frequency pulse-width modulator. Sections a and b form a sawtooth oscillator (of approximately 0.25 Hz), with capacitor C_1 being charged through R_1 and discharged through section a's open-collector output. R_2 and R_3 set the upper voltage limit for the sawtooth wave. The hysteresis means that C_1 is discharged to nearly zero volts, creating a voltage swing identical to the adjustment range of R_3.

Comparator c, in conjunction with

"A great time to introduce a new luxury cruise line. The economy was in a slump, and the competition was on the rise.

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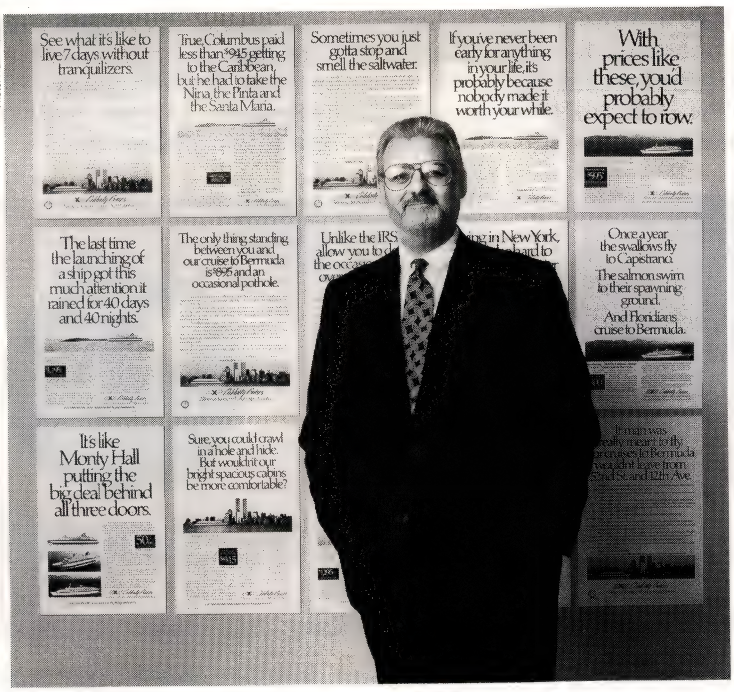
They recommended a three phase campaign. Phase 1. Full page newspaper. One ad a week for 24 weeks and one-third pages in the travel section. Phase 2, radio. Then 3, television to sweep up one season and sow the seeds for the next.

To make a long story short, two-thirds into the newspaper phase, Celebrity's ships were just about full to the end of the season. With so little left to sell, we all agreed to hold the radio and TV and save the remainder of the budget.

In roughly two years Celebrity became the number one cruise line from New York to Bermuda.

We've just added another new luxury ship and we're anxious to fill it. So once again we've upped our budget. So far, our agency hasn't tried to talk us out of it."

Photo: Frank Moscati



Al Wallack, Sr. VP Marketing, Celebrity Cruises, after returning from having his hearing checked.

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This advertisement prepared by Korey, Kay & Partners, New York.

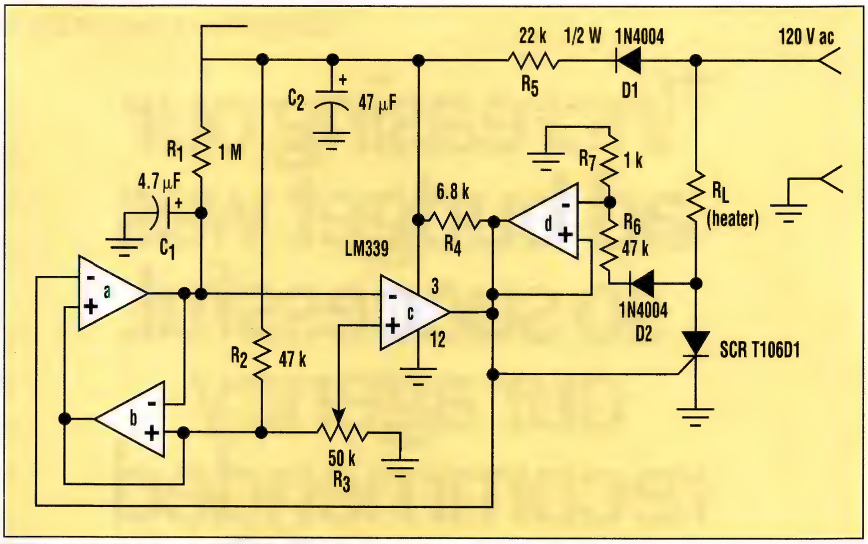
potentiometer R_3, converts the sawtooth waveform to a variable duty-cycle drive for the silicon-controlled rectifier.

Increasing voltage at R_3's wiper means increasing the "on" time. Section d holds the SCR gate low if the line voltage is above approximately 3.5 V, preventing turn on at mid-cycle and ensuring low RFI.

The oscillator frequency is roughly determined by $1/0.7R_1C_1$. Resistor R_1 must be greater than $4R_2$ or the oscillator will lock up. Reducing R_2 will increase the lower voltage limit of the sawtooth; increasing it may cause lock-up.

The nonlinear up ramp isn't objectionable in this application. If it needs better linearity, resistor R_1 may be replaced with a current source or R_3 may be decreased to use a more linear portion of the RC curve. The zero-crossing threshold is set by R_6 and R_7, and by the nominal 60 mV at the comparator's positive input. Any sensitive SCR gate may be used in place of the one shown in the figure. D_1, R_5, and C_2 provide 10 V to power the circuit.

What appears to be a feedback connection from the SCR gate to comparator a's negative input isn't the case. The comparator a needs a voltage between 5 and 0.01 V for a reference, and this point (the SCR gate) provides just that.□



MANUAL CONTROL of the output of a resistive heater or other long time constant load is possible with this low-cost circuit. The device was designed to generate very low RFI.

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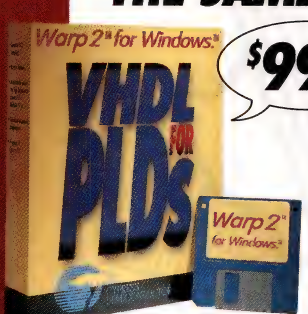

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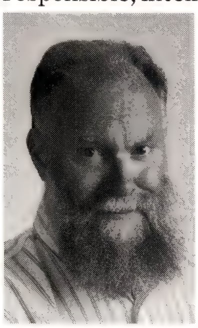
WHAT'S ALL THIS FUZZY LOGIC STUFF, ANYHOW (PART II)?

If you can think of an unlikely person to study Fuzzy Logic, it's RAP. While it's a dirty, nasty job, somebody must do it, and I've had lots of encouragement from all you readers since I put out my first column on the subject.[1] Note, some people have characterized me as being a detractor of Fuzzy Logic (F.L.), but I think I have done more good for the field of F.L. than lots of other guys all put together. I think it's to nobody's benefit to have people bragging about advantages that are unreal.

I believe people who are making responsible, intelligent claims for F.L. will be glad to have me on their side, to cut down on irresponsible, unfair, preposterous claims. I consider myself, rather, a skeptic—and here is a laundry list of ideas I have figured out or discovered so far:



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

1. Nobody has yet submitted to me any realistic task or control loop that they did with Fuzzy Logic which I could duplicate.[2] Isn't it strange that some Fuzzy Logic promoters want to quiet down Pease, but none of them has brought me a nice simple example to show how F.L. really is better than conventional systems (and, after we turn on the lights, we hear them scuttling under the cabinets). I didn't expect to get many, but zero is indeed a very interesting number. However, as one person pointed out, the F.L. experts who really are good are too busy to fool around with demonstrations, since they have lots of work to do—that's a fair explanation.

2. Almost everybody agrees that the examples I gave of outrageous F.L. claims were indeed pretty incredible, and that some F.L. promoters do exaggerate a lot. Several people sent in additional examples of Fuzzy Logic hype, such as pumps that allegedly come up to speed 2 times faster than with a "conventional" controller, and fuzzy motor controllers with miraculous "advantages"....

3. I have seen several readers give the same opinion that F.L. will be a lot more useful and valuable than its detractors predict, but a lot less useful and valuable than its promoters have said. Some of the claims, for example, that 50% of all microprocessors will be used for F.L. by 1996 seem a bit far-out.

4. Some promoters of F.L. are quite young, and when they promote F.L. as superior to other kinds of controllers, they show fantastic advantages—not out of malice, but just because they're not really familiar with the capabilities of other techniques. So they set up a straw man, which they then proceed to knock over easily. They do this because they don't know any better. Those of us who know better have an obligation to explain this to them.

5. Some F.L. guys aren't very good at explaining. Certain people think this may arise from their experiences in applying for research grants: If they clarify everything, and make it look too clear and easy, how can they apply for another grant to explain yet more? Even allowing for this, they still aren't very good at explaining things. They love to use lots of jargon. They speak in terms that are suitable for "preaching to the converted," but don't make clear explanations to the rest of us. Then they bleat that the rest of the world is closed-minded and prejudiced against them. I wonder why that is....

6. For example, some of them like to talk about the ability of their math to handle "probability." When you check it out, you find that they're talking about *proportionality*—the analog parameters. But because many of their old mathematical tools are borrowed from the probability experts, they persist in using that phrase. It bugs the hell out of me!!

7. Many F.L. guys love to make rash, outrageous philosophical claims: "With Fuzzy Logic controllers, you don't need any models." "With F.L., you never have to worry about the Nyquist sample rate." "You do not need to know the characteristics of a plant to design a controller for it." "The major advantage in the use of a fuzzy loop is that it reacts much faster to a process disturbance (or to overshoot and undershoot) than does a standard PID loop."[3] After much debate and criticism from conventional control experts, they may concede their claims aren't entirely true, but only after they have succeeded in getting everybody mad at them.

8. F.L. is claimed to make a good servo for some kinds of systems where conventional controllers don't work well. WELL, let's assume that in some cases it's true. Then how do you prove that such an F.L. system has good dynamic stability in all cases? For conventional controllers, there are methods to prove that a controller has a good safety margin of dynamic stability. How can you demonstrate and prove adequate safety margins/safety factors for F.L. systems? Remember—F.L. claims advantages because it can accommodate system nonlinearity by incorporating appropriate nonlinearity in the controller. How do you prove that this is safe? How much proof is necessary? That sounds like a real problem to me. If your new F.L. washing machine

blows up, how can the manufacturer prove to the jury that he used the best available tests to ensure customer safety? As with any nonlinear controller system, extensive testing is needed to prove that no regions of instability will jeopardize proper system operation.

9. Some people pointed out that a Fuzzy Logic system is a kind of Expert System—a form of Artificial Intelligence. Now, the F.L. people may not like to talk about this because of the disappointments with Expert Systems in the past. But, are these not some of the same people who worked with Expert Systems and Artificial Intelligence in the past?? You tell me. Still, despite old disappointments, this seems to be a place where the Expert System, under the name of Fuzzy Logic, finally begins to fulfill its promise. MEANWHILE, some Artificial Intelligence experts are the most adamant detractors of F.L., because they have their math, and do not like to see F.L. people using "linguistic variables." Personally, if I hear "If the input is *small*, the output is *little*," one more time, I will *vomit*.

10. Let's assume that F.L. really can help make vacuum cleaners and washing machines work better. If that's the case, they do so because of the SENSORS. Which is more important, better sensors or the F.L.?? Maybe those smart, aggressive, and problem-solving F.L. guys will use the sensors very thoughtfully. Which is the chicken, which the egg? I can't say.

11. Fuzzy Logic doesn't really generate a control law. It maps an existing control law from one set of rules into a logic set.[4] If the rules permit this to be done efficiently, it may be able to accomplish the computing function just by remapping. That's a well-known way to get your computation done quickly. But the programmer or rule-maker has to provide the mapping functions —the rules. However, writing those rules isn't a trivial exercise. Even if you want to let Neural Networks write the rules for you, as with NeuFuz4,[5] that can be quite a piece of work.

12. F.L. guys universally ignore the role of their input sensors, their analog-to-digital converters, and the format of the (digital) interface to their Fuzzy Processors. I've heard people say that in some cases, F.L. works just fine with a single input bit stream. In other cases, the controller obviously requires an 8-bit, 10-bit, 12-bit, or higher-resolution parallel data bus. But (just about) every Fuzzy Experimenter makes ZERO mention of the input data. One person admitted about F.L. designers: "*Of course* they need good input data, and they just *assume* that the data will be made available to them in a suitable format."

...Well now, what format is that? It certainly isn't the same for every case, and, therefore, it should certainly be discussed. Every time I've looked at an "example" of a real Fuzzy Logic system or controller, the data inputs were left completely unmentioned. This frustrates the hell out of me because I know that in the real world, in a real system, this is quite important. Caution—don't be fooled into thinking, as one of my friends did, that a F.L. system only needs a 3-bit ADC at its input, because there are only 3 or 4 "rules." These few rules will take in and process the 8 or more bits of data (1 part in 256 resolution), which they then map into an output with full 8-bit (or more) resolution.

Also, don't think that the F.L. process is fuzzy or imprecise, or isn't "deterministic". I have been informed to point out that when the input moves a small amount, the output will move an appropriate amount, with no real uncertainty or doubt. A F.L. controller is, normally, just as "deterministic" as a conventional controller, whether analog or digital. It just uses different internal processes.

The "fuzziness" in F.L. just refers to the way that an object is in a set. In classical set theory, an object is either in a set or it is not. There's no "in-between," no grading. In the real world, of course, objects can be in a set "partially." F.L. extends classical set theory by assigning degrees of membership (typically, fractional amounts) to objects in such a way as to not conflict with classical set theory.[6]

Thus, F.L. can serve as a generalization and as an extension of existing set theory to help solve real-world problems in cases where traditional methods fail, or where nonlinearities cause poor results in price or performance. Of course, many of us engineers use analog signals to represent that proportionality.

13. Note that in most real systems, whether F.L. or conventional, it's important for the system to be given good information, with good resolution and good accuracy. If adequate information isn't made available, it's unclear how either one will do a good job. Specifically, when F.L. guys say that "You never have to worry about the Nyquist sample rate," that is true only if you have a big safety margin. If your F.L. system's sample rate is too low, and your system works badly, then *of course* you have to worry about it, just as everybody else does.[7]

14. In a conventional digital or analog controller, it is customary to provide a parameter, such as distance or rotation, to the controller. The controller then computes a derivative or difference signal, dx/dt, or, $\Delta x/\Delta t$. But in a F.L. system, you have to *provide* the x data and then a derivative, dx/dt. Apparently F.L. falls short when it comes to timing or counting, so the F.L. controller can't compute the derivative function—*you* have to provide it that. Therefore it's *not* quite true that an F.L. system needs the same information as a conventional controller—sometimes it needs *more* information.

15. LIKEWISE, Fuzzy guys uniformly ignore the output format of their systems. Is it serial or parallel? They're always too shy to mention this. I did hear that for the Inverted Pendulum experiment, the F.L. approach is so greatly superior to conventional controllers that it puts out just a serial pulse train (the signal is the duty cycle) which controls the loop without any trouble. Yet in other cases, it's obvious that the output must comprise parallel bits to a conventional DAC. But they never make any reference to this, either. How many bits, 8, 12, or 16? Nobody talks about this; it's "academic" and is left as an exercise to the reader.

16. Not only do the F.L. guys never talk about their input interface or their outputs, they also avoid talking about the actual computer or micro-

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processor they use. They rarely mention the number of bits, or the clock rate, or the software. They always try to keep things "academic"—and they don't tell you what they really did.

NOW, let's talk about cases where F.L. may have advantages:

17. Fuzzy Logic is generally admitted—even by RAP—to have real advantages where the system is nonlinear. One simple example, again, is the Inverted Pendulum, where the base of a stick on a pivot is moved along a track by a little motor. The angular acceleration of the pendulum is NOT a linear function of its angle away from vertical, but a sort of third-power law. If you try to approximate this with a linear function, it's hard to get the gain right. It's either too low at the ends or too high in the middle. Or else you have to compute the function precisely, which takes a LOT of computation. But with F.L., you can get the gain approximately right with just a few segments of F.L. coding—perhaps just 5 rules. These rules now are so simple, that the F.L. computing processors can compute this with good speed, and a cheap computer, faster and cheaper than a conventional computer can do when it computes EXACTLY the equations of motion for that Inverted Pendulum. Consequently, if the computer can go faster, it may be able to do a superior job of controlling, because although its math is crude, it's plenty accurate enough, and it's *fast*. NOW, when you compound the problem by stacking *two* inverted pendulums on top of each other, F.L. can still do it easily. For the *triple* inverted pendulum, F.L. can still do it, whereas conventional controllers apparently can't do all of the complicated math fast enough. *Maybe* if you made some simplifying assumptions, some approximations, the conventional controller could then go fast enough, but this is generally ignored. F.L. can make certain assumptions, approximations, and simplifications, but other controllers aren't supposed to be able to do this.

18. F.L. is supposed to have real advantages where an approximate system solution is adequate. For example, I read a statement by a F.L. promoter[8] that said if you want a computer to park your car for you, you should exploit imprecision. If you don't need the car at exactly 6.00 ±0.02 inches from the curb, but something like 6 ±2 inches, then F.L. may be able to do a superior job, especially since you can use a cheap computer. When I read this, I was struck by its wisdom. But who would dare to admit that F.L. is not only not always better, but sometimes, *inferior* in accuracy, yet it's still plenty good enough? I looked, and it was Lotfi Zadeh himself, the creator of Fuzzy Logic. He was wise enough to say that, and I'm delighted to say I agree that when a solution is good enough, don't worry about perfection. I'm absolutely in favor of pragmatism, and of good-enough engineering. Perfectionism is the bane of cost-effective engineering. Anybody who knows when to do a good-enough job and *stop* is a friend of mine.

19. Let me insert an esaeP's fable here: One time I was bicycling down Massachusetts Avenue in Cambridge, Mass. on a quiet Sunday morning, and a dog started chasing me. Because I was on a downgrade I accelerated well, and the dog fell a few yards behind me. He could not gain on me, and I was going fast enough, so I did not bother to pull further away from him. At a split in the road, I continued on down Mass Ave. The dog veered off onto Mt. Auburn Street, barking all the way, as if to say that he was not really chasing me at all, so he did not care if he had not caught me.

WELL, when I make a few convincing arguments to rebut the F.L. claim that "F.L. is always better", the F.L. experts often veer away, saying, "Even if it is not always more precise, it is less expensive...." NOW, F.L. is *alleged* to be a less expensive way to run a controller. In some cases, it may be able to use a cheap computer. It may use fewer lines of code or a smaller ROM. The F.L. guys love to claim this. But I don't automatically trust them when they say "it's cheaper." After all, what would you expect them to say?? I am still skeptical about these guys. Other experienced engineers find that for some cases, *conventional* controllers can be more compact, cheaper, and easier to program than F.L. So, if in a given system the F.L. experts claim that F.L. is cheaper, you had better check their data. Make your own cost comparisons. Don't let them just set up straw comparisons.

Stay tuned for more Fuzzy Logic stuff in the next issue...

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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Santa Clara, CA 95052-8090

References:

1. "What's All This Fuzzy Logic Stuff, Anyhow?," R. A. Pease, *Electronic Design,* May 13, 1993, pp. 77-79.

2. One reader sent a report on a design involving a focusing system for a laser's lenses, but I couldn't very well duplicate that. Another person promised to send me more info about a motor speed controller, but never sent anything. One writer said that "all of the arguments of the above writer are not right," but gave no specific example of anything in my writing he thought was wrong....

3. "Fuzzy Logic: A Clear Choice For Temperature Control", Haubold vom Berg, *Instruments and Control Systems,* June 1993, pp. 39-41.

4. Private correspondence with Daniel Abramovitch, Hewlett-Packard Labs, Palo Alto, Calif. June 30, 1993.

5. NeuFuz4 from NSC, combining Neural Networks and Fuzzy Logic. The Neural Network part can learn from recorded data, then generate fuzzy rules and membership functions. Thus, it can learn the best way to control the system. Call (800) 272-9959 for details.

6. "Fuzzy Models - What Are They, And Why?" J. Bezdek, IEEE Transactions on Fuzzy Systems. Feb. 1993, pp. 1-6. A good introduction to Fuzzy Sets and concepts.

7. Private correspondence with Daniel Abramovitch, Hewlett-Packard Labs, Palo Alto, CA. June 30, 1993.

8. "On The Fuzzy Edge Of Technology", Tom Williams (quote of Lotfi Zadeh), *Computer Design,* April 1993, p. 14.

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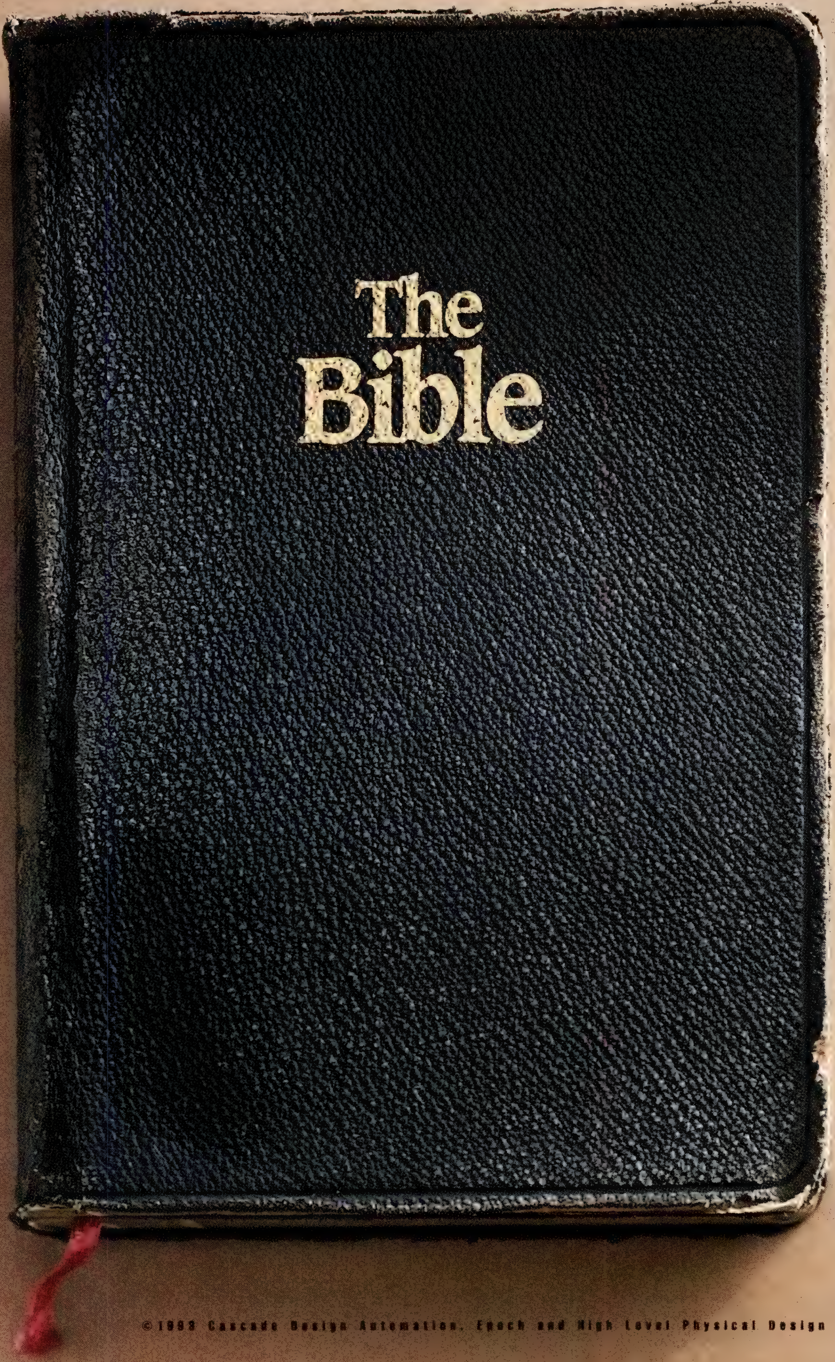

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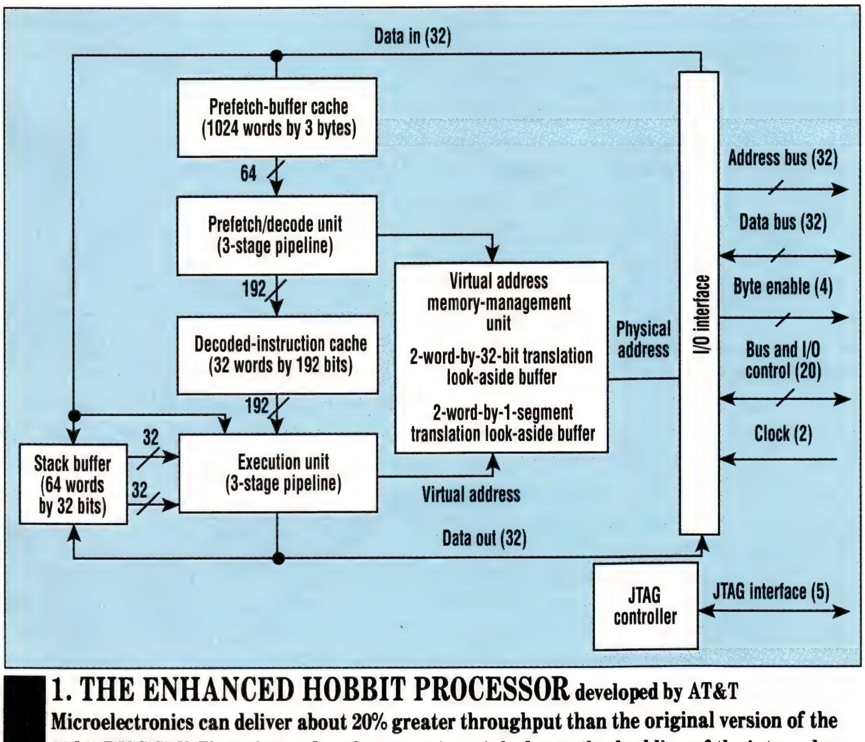
Similar demands for just-emerging personal communications assistant/personal digital assistant (PCA/PDA) products led designers at AT&T Microelectronics to create three second-generation Hobbit-family CPUs and related support chips. The three families will give PCA/PDA designers the opportunity to craft a range of products, from limited-expandability, dedicated-function handheld units to very flexible, reconfigurable systems.

The three second-generation CPUs are upwards software-compatible with the original 32-bit Hobbit processor, the ATT92010. Each of the CPUs share the C-optimized RISC-like processor architecture introduced in the ATT92010. With enhancements to the architecture, though, the ATT92020S, the highest-performance member of the three, can deliver a peak performance of 16 VAX MIPS when running at 20 MHz and 3.3 V, equivalent to a performance/power rating of 76 MIPS/W. When powered from a 3.3-V supply, the original Hobbit delivers a throughput of 13.5 MIPS, as well as 27,000 Dhrystones, at a clock of 20 MHz.



1. THE ENHANCED HOBBIT PROCESSOR developed by AT&T Microelectronics can deliver about 20% greater throughput than the original version of the 32-bit RISC CPU. The enhanced performance is mainly due to the doubling of the internal prefetch buffer cache's size to 6 kbytes.

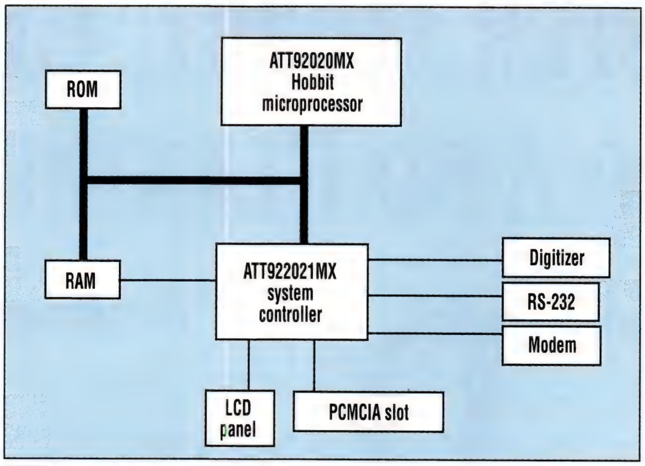
The performance/power ratio of the 92020S is roughly two to five times greater than what's offered by the 80386- or 80486-family processors. The other two CPUs, the 92020M and 92020MX, deliver peak performance levels of 13.5 and 11.5 MIPS, respectively, and will also operate at 20 MHz maximum (at 3.3 V). All three CPUs, however, employ the same CMOS static logic design that was applied to the 92010 CPU, which consumes just 360 mW maximum (typically 250 mW).

To achieve that throughput, the processors, like the 92010, rely on branch prediction, branch folding, and hazard detection/bypassing to reduce the overheads associated with program branches and data dependencies. These schemes also eliminate the need to employ "band-

aid" approaches, such as delayed branches and load-delay slots, which are really meant for inefficient code that uses large basic blocks.

Even though the Hobbit processors are optimized for 3.3-V operation, they can also perform at 5 V. Power drain does increase, but that's offset by a 50% boost in throughput, enabling any of the three CPU chips to operate at a maximum clock speed of 30 MHz.

At 20 MHz and 3.3 V, the power consumption for the 92020S typically runs about 210 mW. The M and MX versions will consume slightly more due to their multiplexed address/data buses—250 and 290 mW—and have efficiency ratings of 54 and 40 MIPS/W, respectively. In their sleep modes, the processors will draw only about 50 μW. However, at the system level, the power consumption ranges from 490 mW for the 92020S with its basic support chip set (the same support chips as used by the ATT92010), to 530 mW for the 92020M and its two dedicated support chips, and down to 390 mW for the 92020MX with its lone highly integrated support chip.



2. A VERY COMPACT SYSTEM can be built with the AT92020MX Hobbit CPU and its companion support chip, the 92021MX. Between the two chips, all of the system logic needed for a handheld computer is integrated, including the display controller and a controller for one PCMCIA slot.

Larger Cache

To improve the CPU's performance, the size of the three-way set-associative cache on the 92020S and 92020M was doubled to 6 kbytes, while the 256-entry stack cache and the 32-entry decoded-instruction cache were kept the same size as the original 92010 *(Fig. 1)*. The ATT92020S is directly pin- and software-compatible with the 92010 and can thus be used as a direct upgrade for existing designs.

Furthermore, because the 92020S can drop into the same 132-lead 92010 pad sites, it can use the identical set of support circuits released last year: the 92011 system controller, the 92012 three-channel PCMCIA controller, the 92013 auxiliary I/O interface (ISA expansion bus), and the 92014 video controller (ELECTRONIC DESIGN, *Oct. 15, 1992, p. 92)*. In addition to the 132-lead PQFP package, AT&T will offer the 92020S along with the other two new CPUs in space-saving 144-lead thin plastic quad-sided flat packages.

A second enhancement to the overall CPU is a new "Wait for Interrupt" instruction that eases the integration of operating-system and power-management capabilities. Other changes on the M and MX versions include the change of signal polarity from active low on the 92010 and 92020 CPUs to active high on the M and MX. Such a change improves the ability to perform automatic status checks and greatly reduces the amount of drive current needed to maintain signal levels. The active-high approach matches the signaling well because powered-down devices would indicate an inactive state with a low signal level (0 V). That low level simplifies control schemes and eliminates the need for the use of active pull-up circuits.

Software-controlled clocks are another feature of the 920X0 family. They help the CPUs manage event-driven power-up sequences. The PenPoint operating system, developed for use with the Hobbit, takes full advantage of the clock-control capabilities because it gives the operating system the ability to dictate the power-down sequences. PenPoint does this by interacting with the control logic and sending one of four power-status messages to the power-manager section. Those four messages—Full Power, Idle Power, Standby, and No Power—tell the manager which call to make to the machine-interface layer of the software. The manager then interacts directly with the chips, turning the appropriate clock signals on or off whenever needed.

For more highly integrated but perhaps less flexible systems, the 92020M and MX Hobbit processors change the CPU pinout from separate 32-line address and data buses to a single, multiplexed, 32-bit address/data bus. That frees up 32 lines. But instead of reducing the chip pin count, AT&T's designers used those pins to provide latched address signals. Those latched signals can be used by external ROMs or I/O devices.

Furthermore, to reduce the number of chips in a 92020M-based system, AT&T's designers combined the PCMCIA and system-controller functions onto one chip, the ATT92021M. They also created an enhanced video controller, the 92024M. Both the ATT92021M and 92024M chips tie into the multiplexed address/data bus.

The PCMCIA sub-block in the 92021M system controller handles two card slots, rather than the three possible with the 92012. Furthermore, the system controller offers the same power-management and memory-control functions as the 92011 system controller. One extra enhancement is that the 92021 system controller gives users a choice of either a 16- or 32-bit ROM data path, which provides more flexibility in memory-subsystem design.

Serial Port

Additional functions on the 92021M and MX versions include a 3-wire serial port compatible with National Semiconductor Corp.'s MicroWire interface. This popular 3-wire interface can be used to tie into a wide variety of serial peripheral chips—RAMs, nonvolatile memories, analog-to-digital converters,

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etc. Consequently, they provide a wide range of simple I/O functions for Hobbit-based systems.

However, for the compact systems that are expected to use the M and MX families, AT&T designers decided to remove the keyboard interface from the 92021. Most systems will probably use a pen-input rather than a keyboard to capture information. The 920X1 chips also include 256 bytes of low-power RAM featuring its own power-supply interface so that it can be backed up by an external 3-V lithium cell. The RAM holds system state information (such as real-time clock settings, power-control information, machine IDs, and so on).

The 92020M and MX use the same CPU core as the 92020S. As a result, even with the multiplexed bus interface, they can deliver performance comparable to the 92010 and still consume about the same power. For video support, the 92024 video controller provides up to nine bit planes (512 colors) with resolutions as high as 1024 by 768 pixels, and support for both LCD and CRT displays..

MAXIMUM INTEGRATION

For maximum integration at the lowest cost, the 92020MX drops back to a 3-kbyte on-chip cache. Moreover, the supporting system controller, the 92021MX, handles all system control, PCMCIA, and display functions, reducing the chip count to just two circuits (not counting memory and application-specific I/O functions) *(Fig. 2)*. Just one PCMCIA card is supported by the 92021MX. The simplified display controller delivers a maximum image of 640 by 480 pixels. Combined, the two chips typically consume just 390 mW when in the active mode and about 100 μW in the standby mode.

All three CPUs and the support chips include IEEE 1149.1 JTAG test ports, which simplify on-board testing of the circuits. This eliminates the need to add area-consuming test points to the limited area of circuit boards used in PCAs and PDAs. The 92020S will come in either a 132-lead plastic quad-sided flat package as a direct-replacement for the 92010, or in a thin, 144-lead quad-sided package. The 92020M and MX will also be available in 132-lead PQFP and 144-lead TQFPs. All of the support chips come in 208-lead shrink PQFPs, which minimize board area.

SUPPORT TOOLS

Software support is in the form of the object-oriented PenPoint operating system. It features a pen-and-paper, notebook-style user interface that can translate handwritten input into text or graphics in real time. PenPoint readily scales from pocket-size to clip-board-size personal systems, automatically adjusting the user interface to fit the screen. Moreover, it includes integrated power-management capabilities to minimize system power.

Software development tools for the Hobbit family have been available since last year. Except for the new Wait-for-Interrupt instruction, all software tools can be used to develop new application programs. A revised set of tools will be available later this year. Evaluation tools start with a standalone personal-communicator development system and include a symbolic debugger that runs under Windows 3.1, a real-time in-circuit debugger, and an HP 16550 logic-analyzer interface. The development system consists of two units—an EO Inc. personal communicator and a docking station that holds four PCMCIA slots, an IDE disk-drive interface, a serial port, and four ISA bus slots.☐

PRICE AND AVAILABILITY

All three enhanced Hobbit CPUs and the new support chips will be ready for sampling later this year. Prices for the CPUs start at $32 each for the ATT92020MX, and increase to $34.50 and $37 apiece for the 92020M and S, respectively. Support chipset prices, including the CPU, range from $63/set for the 92020MX and 92021MX, and increase to $80/set for the 92020M, 92021M, and 92024M. Finally, the 92020S, the 92011, 92012 and 92014 go for $101/set. All prices are for purchases in lots of 10,000 units or sets.

AT&T Microelectronics, 4995 Patrick Henry Dr., Ste. 2000, Santa Clara, CA 95054; Rakesh Sood, (408) 980-3780.

CIRCLE 524

HOW VALUABLE?	CIRCLE
HIGHLY	550
MODERATELY	551
SLIGHTLY	552

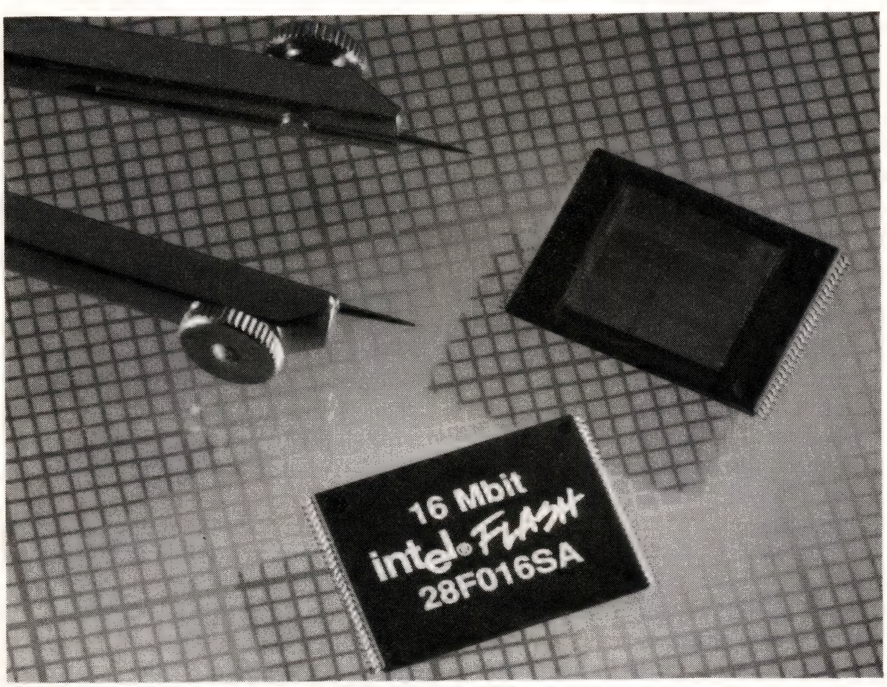
16-MBIT FLASH CHIPS RAISE THE CAPACITIES AND PERFORMANCE OF MEMORY CARDS AND ATA SOLID-STATE DISK DRIVES.

PORTABLE-SYSTEM USERS CAN TAKE 40 MBYTES ON THE ROAD

RICHARD NASS

Portable computers represent one of the hottest areas in the industry, particularly if you go by sales figures. But that growth has also brought about new demands for lighter, higher-capacity, lower-power, and more rugged methods of data storage. One method engineers have turned to is flash memory.

Though flash memory isn't new, its low capacities, fairly slow access times, and high cost have made it somewhat prohibitive. Nonetheless, in many small handheld computers, called personal digital assistants (PDAs), flash memory is used as the primary storage medium. Flash also shines when it comes to upgradability. On a portable or desktop motherboard, flash chips can replace EPROM for BIOS retention. As a result, the BIOS becomes a user-upgradable option.



1. TWO DIFFERENT FLASH MEMORIES, developed by Intel and Sundisk, can each store up to 16 Mbits of data. The chips can be used for mass storage as flash cards in a PCMCIA-compatible form factor.

Recently, two announcements have given flash memory an even greater boost: Now users can get the capacities and performance they require at a price that should fall to an affordable level. The two devices, from Intel Corp., and SunDisk Corp., both of Santa Clara, Calif., can store up to 16 Mbits of data.

Each company manufactures the flash chips, but only Intel will sell them in IC form. SunDisk will put the chips into PCMCIA-compatible ATA flash cards, then sell those cards either with their own label or under a third-party label. Intel also will sell flash cards, or even an ATA card, which is viewed by the system as if it were a rotating-media hard-disk drive. As a result, designers can use the Intel chips for BIOS retention.

All of the flash cards offered fit the PCMCIA form factor. The Intel flash card fits the Type 1 (3.3-mm high) form factor, while its hard-drive card and SunDisk's card are

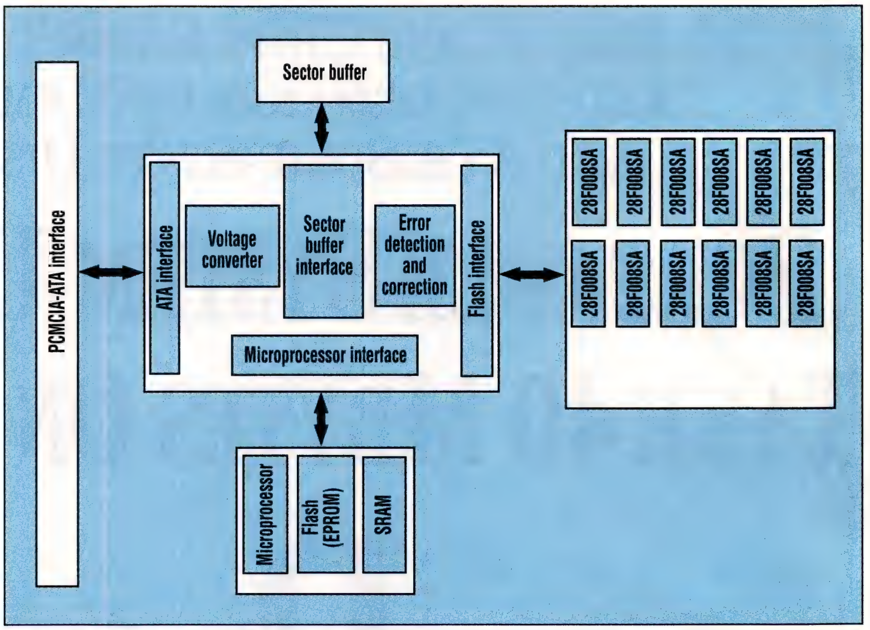
Type 2 (5-mm high) models.

Intel's flash technology, dubbed ETOX IV for EPROM Tunnel Oxide, is carved with 0.6-μm lithography while SunDisk's parts are made on a 0.5-μm process. Intel's 28F016SA chips, a fourth generation of the ETOX family, can operate at either 3.3 or 5 V *(Fig. 1)*. They handle up to 1 million write cycles before failure, while an infinite number of reads can be made. The 3.3-V version offers a 40% power savings over the 5-V part. When installed in a card, a signal pin is available to differentiate between 3.3- and 5-V devices.

Intel's 16-Mbit flash ICs have improved performance over the previous generation of 8-Mbit parts. For example, the 16-Mbit chips offer an access time of 70 ns (at 5 V), while the earlier chips offered access times of 80 ns. At 3.3 V, the access time is 120 ns. The new parts are built with an on-chip 512-byte page buffer (two 256-byte buffers). This permits 512-byte blocks of data to be written at the speed of the system's RAM. The maximum throughput rate on write operations is 1.7 Mbytes/s, a four-times improvement over the 8-Mbit parts. Also, the chips can be configured as 2 Mbits by 8 bits or 1 Mbit by 16 bits for maximum flexibility.

Intel's 16-Mbit components feature block locking on every block. With this capability, one bit per block can be set to prevent writing to that block. Any of the 32 (16 on the 8-Mbit chip) 64-kbyte blocks on the device can be locked. Locking the top or bottom block of the chip can turn it into a boot-block device. This means that it can hold the boot-up code, which the manufacturer wouldn't want users to alter. Another way to use the block-lock feature is when developing application code. This can be a significant feature for memory-card makers who prefer, for example, to offer some software on the card.

The 28F016SA parts are built with a command queue that permits more than one command to be queued up. In some cases, multiple commands can be executed at one time—it can write during an erase cycle. Write operations can occur in one block while an erase operation is taking place in another. If the system tries to write to the same block that's being erased, it will stop the erase operation, begin the write process, then pick up the erase operation following the write in another block. A Ready-Busy pin tells the host CPU when a task is complete. This means the host need not constantly poll the system, and is offloaded from monitoring some of the operations.



2. THE ATA FLASH DRIVE designed by Intel contains an on-board local microprocessor that executes card-resident controlling firmware, similar to a rotating drive's controller. The card provides a maximum capacity of 10 Mbytes.

The flash card differs from the ATA flash drive in that it relies on the host system to manage the media through a software flash-file system that resides on the host. Consequently, there's less overhead software to manage the media in the card, yet more in the system, resulting in a lower-cost card.

Intel's flash cards offer a direct-execute capability, meaning that applications can run directly from the card without having to download the data to the system's main memory—it's executed directly from the card to speed up the operations. The cards are offered in 4-, 20-, and 40-Mbyte capacities.

One benefit derived from a lower-capacity card, such as a 4-Mbyte card, is that it comes with a lower price tag than a rotating-media drive. There's a definite floor to hard-drive cost because, regardless of capacity, a motor, read/write heads, media, etc., are needed. Flash cards don't carry this extra baggage.

The Intel flash cards have a 200-ns access time at 5 V and 250 ns at 3.3 V. They fit into either a 3.3- or 5-V system. Built-in intelligence detects the system's voltage level.

The ATA flash drives designed by SunDisk, named the SDP5A-40, hold up to 40 Mbytes in a Type 2 form factor (the Intel ATA cards hold up to 10 Mbytes). Lower capacities are also available. The company says that using 16-Mbit components will drive down flash-card prices because twice as many chips can be produced from 16-Mbit die wafers, compared to the 8-Mbit wafers. The write-transfer rate is 75 kbytes/s, while reads occur at 1 Mbyte/s.

The drive is compatible with both 5- and 12-V systems. It has a tested endurance capability of up to 10,000 insertions and 200,000 cycles, which translates to more than 250 years of typical mobile computing, claims the company.

Cards from both companies operate at altitudes of up to 40,000 ft. and can handle operating and non-operating shocks of up to 1000 Gs. Error protection is built into each sector on the card to maximize data integrity.

Password security is built into the SunDisk card. Users can select a security password to protect their

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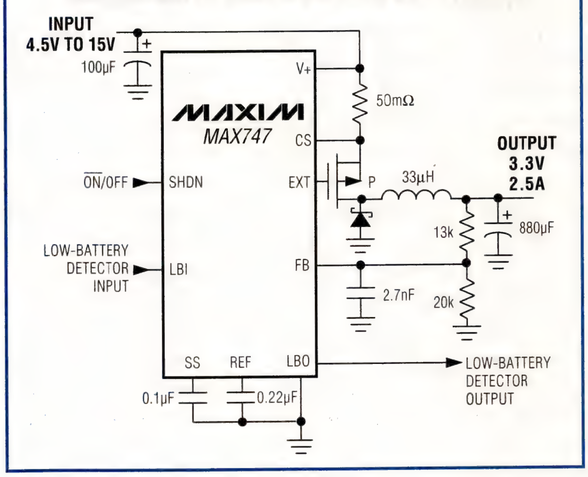

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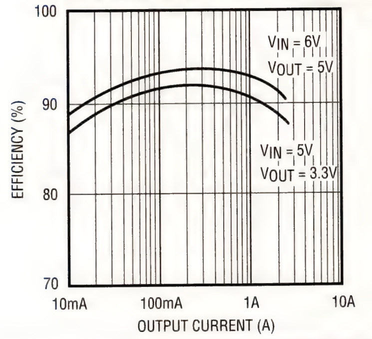

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*1000up, US recommended resale

CIRCLE 162 FOR U.S. RESPONSE CIRCLE 163 FOR RESPONSE OUTSIDE THE U.S.

data. If the card should become lost or stolen, the data remains secure because the password is needed to access the data. Another feature of the card is its power management. A good portion of the time, the card is asleep and drawing almost no power. Peak power is programmable, set by the system's BIOS, with a maximum current of 100 mA.

Intel's ATA flash drive contains an on-board local controller that executes card-resident controlling firmware, identical to a rotating drive's controller *(Fig 2)*. This increases the product's cost. The drive employs the same 68-pin edge connector as the flash card, but it fits a Type 2 form factor. The initial offerings hold 5 and 10 Mbytes using Intel's 8-Mbit chips and an IDE interface jointly developed by Intel and Conner Peripherals, San Jose, Calif.

The drive's capacity can be doubled using commercial compression software, just as if it were rotating media. Its under-1-ms access time compares favorably with the 10 or 12 ms for typical high-speed rotating-media drives. The card is built with an integrated filing system. This means that when the system asks for a data block, the local controller goes through its data and extracts the information. The sustained transfer rate is 6 Mbytes/s.

By employing power-management features, components that aren't in use can be shut down. The host can also initiate some low-power modes, such as a sleep mode. Or, the drive can initiate power management itself using standby idling with instant turn on. The advanced power-management features contribute to a power specification that's about twenty times lower than a typical rotating-media drive.

Because the flash drive has no read/write head that's required to move across a disk, it offers zero latency. While the read transfer rate is 6 Mbytes/s and the card writes at 0.27 Mbytes/s, for small amounts of data, the absence of any latency means the write speed can be faster than that of a rotating hard drive.☐

PRICE AND AVAILABILITY

The SunDisk 40-Mbyte SDP5A-40 ATA card is sampling now for $985 each. It will ship in full volume in the second half of 1994. Intel's 28F016SA flash chips are sampling now, with production of the chips and the 40-Mbyte flash card commencing sometime in the fourth quarter of this year. The ATA card will sample in the fourth quarter, followed by production quantities in the first quarter of next year. The chips cost $94 each in quantities of 10,000. The 40-Mbyte flash cards cost $2200 each and the 10-Mbyte ATA cards cost $475 apiece, both in 1000-unit lots.

SunDisk Corp., 3270 Jay St., Santa Clara, CA 95054; (408) 562-0500.

CIRCLE 517

Intel Corp., 2200 Mission College Blvd., Santa Clara, CA 95052; (800) 548-4725 or call your local Intel sales office.

CIRCLE 518

HOW VALUABLE?	CIRCLE
HIGHLY	544
MODERATELY	545
SLIGHTLY	546

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(Required by 39 U.S.C. 3685)

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2. Mail Subscription *(Paid and/or requested)*	169,318	168,967
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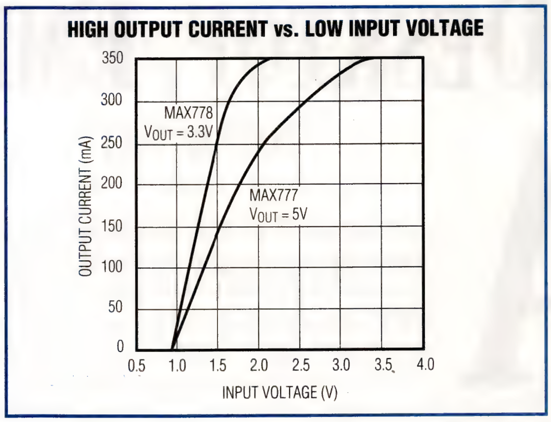

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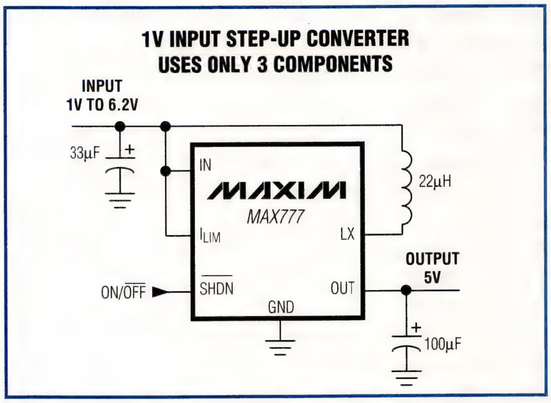

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Packing A Full 64-Bit Architecture, A RISC CPU And Its Support Chips Form Compact Desktop Or Embedded Systems.

Speedy RISC CPU Fits NT Desktop, Embedded Needs

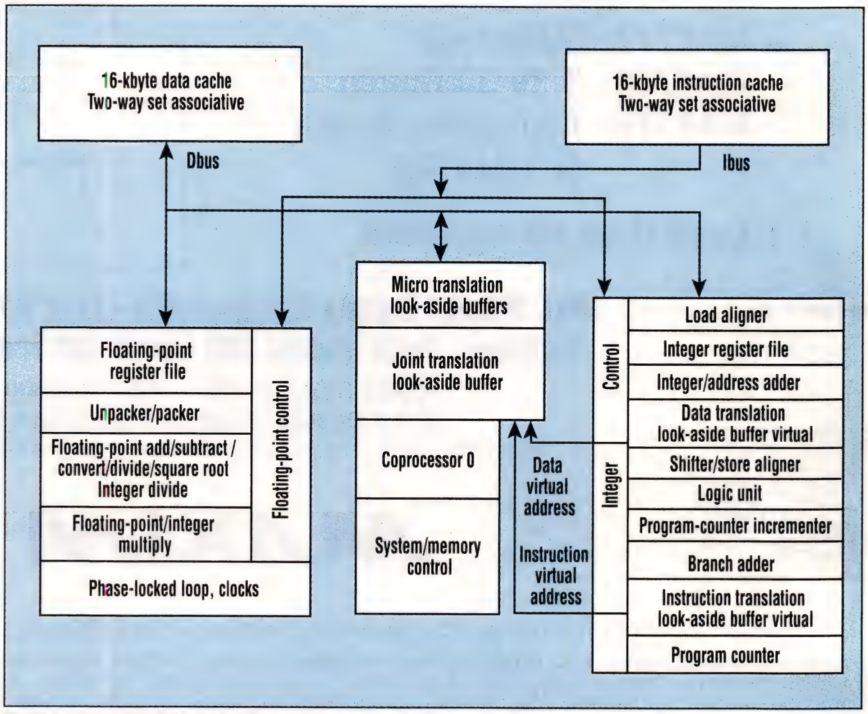
Dave Bursky

As embedded-control applications demand higher CPU performance and integration levels, CPU design requirements are converging with the system needs of the desktop computer. The growing similarity of CPU and system needs—low cost, high integration, low-to-moderate power consumption, and high throughput—was what brought Integrated Device Technology; Quantum Effects Designs Inc., Santa Clara, Calif.; and Toshiba America Electronic Components together. The result of their joint efforts is the R4600, a 64-bit RISC microprocessor (previously referred to as the Orion) and a set of support chips.

The CPU and chip set will simplify the design of high-performance desktop computers compatible with Microsoft's Windows-NT or Unisoft's Unix V.4 operating systems, deskside or departmental servers, and embedded control systems. And, because the chips are signal-compatible with other R4000 processors, Toshiba's Tigershark two-chip set can be used to form NT-compatible systems. Furthermore, a second chip set (code-named Mako), which will provide a PCI-compatible bus interface, is under development and should be available in the first half of 1994.

The 64-bit processor, which is an extension of the MIPS R4000 architecture, will initially be available with an internal clock speed of 100 MHz (50 MHz external). However, the architecture and process will eventually let the internal clock speeds reach 167 MHz. An on-chip phase-locked loop doubles the input clock frequency up to the desired value, and also delivers a 50-MHz output that provides synchronized timing signals for the rest of the system.

At 100 MHz, the processor has an estimated integer throughput of about 68 SPECint92 and can hit peak



1. WITH DOUBLE THE AMOUNT of cache as the R4000PC, the R4600 RISC processor produced by Integrated Device Technology and Toshiba provides designers with a full 64-bit architecture. The CPU runs at a 100-MHz internal clock and delivers an integer throughput of 68 SPECint92.

instruction execution rates of 100 MIPS. The processor's bus bandwidth of 400 Mbytes/s at 100 MHz (internal clock) makes the chip particularly attractive for high-throughput embedded applications, such as those found in networking and data communications systems.

The on-chip floating-point coprocessor has performance comparable to most other RISC CPUs. That includes floating-point math units with a 60-SPECfp92 rating, and a peak throughput of 33 MFLOPS. The FPU has a separate multiplier and a combined add/convert/divide/square-root unit, permitting the section to overlap multiplications and additions/subtractions. The multiplier is partially pipelined, allowing a new multiplication every 6 cycles.

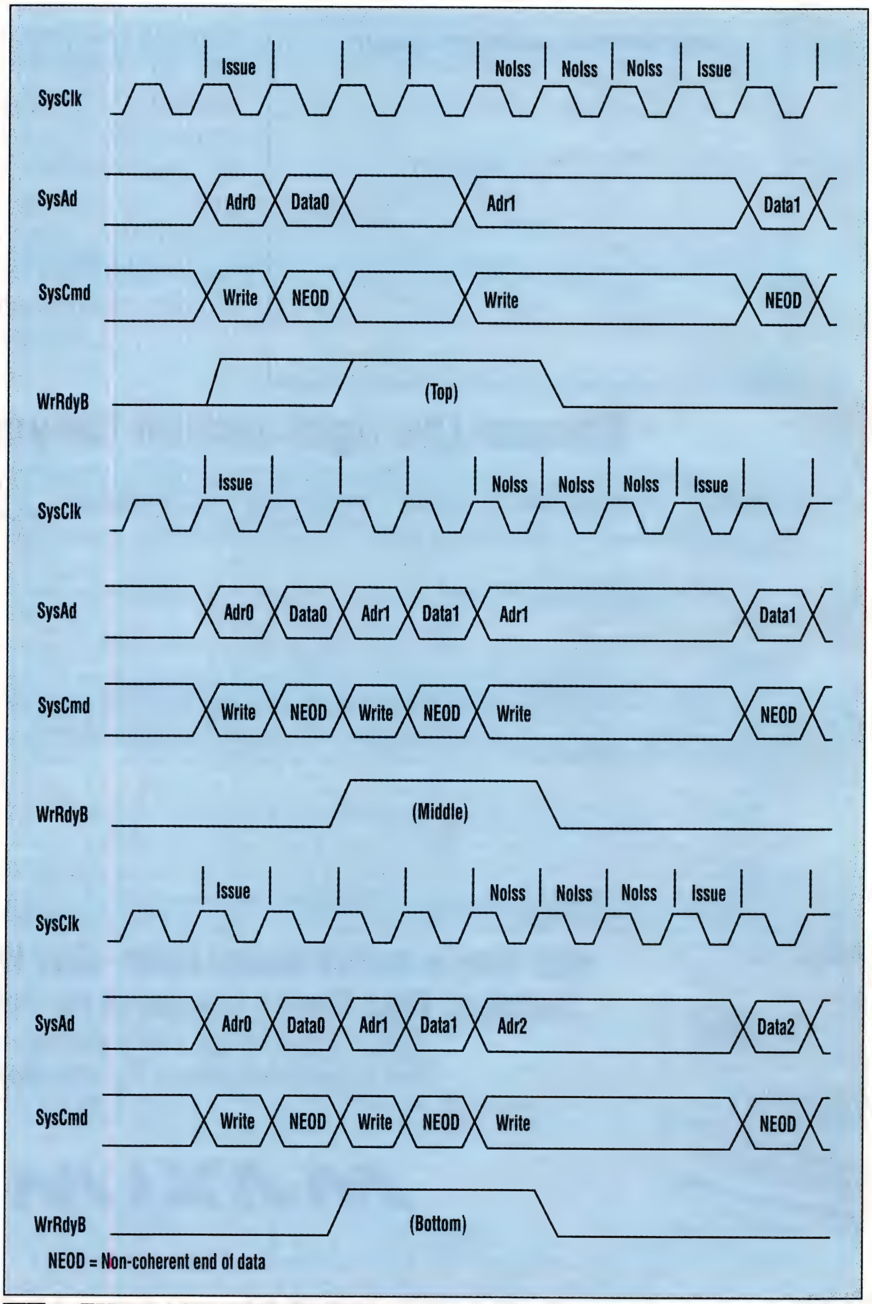
To save chip area, integer multiplication and division are performed by sharing the floating-point hardware, rather than providing the integer ALU with a separate multiplier. To achieve the high throughput rate, the processor takes advantage of a large amount of on-chip write-back cache—16 kbytes each of data cache and instruction cache, which are both two-way set associative with 32-byte line sizes *(Fig. 1)*.

On the data cache, the CPU can request the desired double-word first and then restart when it arrives, refilling the rest of the cache line in the background. As a result, a typical instance could save a minimum of 7 external or 14 internal clock cycles each time the cache retrieves a data line from external memory. Such an option, however, provides no benefit for the instruction-cache operation since instructions are most often retrieved from sequential addresses.

Moreover, the processor was designed as a "true" 64-bit CPU: It handles 64-bit integer and floating-point operations, includes 64-bit registers, and provides a 64-bit virtual address space. To manage that address space, the CPU incorporates a flexible memory-management unit and a large, fully associative, translation-lookaside buffer (TLB) that maps 96 virtual pages to their corresponding physical addresses. Smaller TLBs, a 2-entry instruction TLB and a 4-entry data TLB, map 4-kbyte pages to each table entry.

The 64-bit computing and addressing capability of the processor opens up a wide variety of capabilities heretofore limited by the smaller address space of previous R4000-family members. For example, the large address space allows operating systems to do extensive file mapping and directly access large files without explicit I/O calls. Applications such as large CAD data bases, multimedia software, high-resolution image storage, and retrieval can all benefit from a large address space.

In addition, the arithmetic unit uses a simple five-stage pipeline that keeps latencies low and minimizes the penalty if the pipeline is broken.



2. THE BASIC BUS TIMING on the R4000PC has two null cycles as part of its four-cycle bus transfer (top). By using those two null cycles to issue a second address and a write command, the R4600's write-reissue bus transfer doubles the bus-transfer speed (middle). Pipelined writes start out the same as Write Reissue cycles, but change after the fourth clock when Address 2 is placed on the System Address bus and a Write command is given (bottom).

In contrast, the R4000 employs an eight-stage pipeline. Virtual-to-physical address translation in the new R4600 is done in parallel with the cache accesses. That allows the CPU to run at twice the frequency of the R3000 and support a larger TLB for address translation.

As part of the address mapping, the processor provides three modes of virtual addressing—user, supervisor, and kernel. These mechanisms let the system software provide a secure environment for user processes. Bits in a status register determine which virtual-addressing mode is used. In the user mode, the CPU provides a uniform virtual-address space of 256 Gbytes (2 Gbytes in its 32-bit mode); in the kernel mode, four distinct virtual-address spaces totalling 1024 Gbytes are simultaneously available; and in the supervisor mode, three regions of 256.5 Gbytes of virtual space is available.

For fast virtual-to-physical address decoding, the R6400 includes a large, fully-associative TLB that maps 96 virtual pages to their corresponding physical addresses. It's organized as 48 pairs of even-odd entries, and maps a virtual address and an address-space identifier into the 64-Gbyte physical-address space.

The integer portion of the processor includes 32 double-word (64-bit) registers, a pair of 64-bit multiply/divide registers, and a 64-bit program counter. The floating-point portion of the CPU delivers IEEE-754-compatible single- or double-precision results, and operates in parallel with the integer unit. Non-cached writes can be done quickly as well as on the chip. A 4-double-word-deep write buffer enables the CPU to write to memory and continue its work while the actual writes take place in the background.

To improve the way the processor communicates with memory, designers at QED created a new bus protocol that transfers data with just a two S-clock cycle. Standard R4000-compatible transfers using a four S-clock cycle can also be performed, minimizing the amount of redesign needed when systems are upgraded. A new Write Reissue protocol that eliminates two null cycles between writes was also implemented on the processor. In addition, pipelined writes can be done while still maintaining the R4000 write-issue rule (the protocol simply eliminates the two null cycles between writes). However, to do that, external hardware is required to buffer the pipelined address and data *(Fig. 2)*.

But even with the large amount of cache and the 64-bit architecture, the chip size is only about half that of the R4000 CPU, making the chip exceptionally cost-effective. The R4600, though, will be signal-compatible with the R4000PC chip and yet will deliver more than twice the integer throughput of an i468DX2-66, and about 50% more than the Intel Pentium processor. If upgrading from an R4000 system, the R4600 can use some of the same configuration information and the operating-system hardware abstraction layer. However, cache-related routines must be modified to support the two-way set-associative caches in the R4600.

To keep the chip area small, designers at QED had to forsake some features—the R4600 doesn't directly support a secondary cache, or multiprocessor systems, or a master/checker architecture. Although direct secondary cache support is not included, secondary caches can be implemented with off-chip logic. However, for most applications, the on-chip caches should make the secondary cache unnecessary.

Further simplifications include the use of just one parity bit per 32 data bits in the instruction cache, no JTAG in-system test support, no dynamic feedback or slew-rate control on the I/O pins, and no Watch register (no hardware address breakpoint). To maintain compatibility with previous R4000-family chips, the R4600 does have JTAG data input and data output pins. However, they're internally shorted and thus the chip can be included in a scan chain, but all incoming patterns are sent through to the next chip.

Designed with fully static CMOS logic, the R4600 can run at either 5 or 3.3 V, with Toshiba offering only a 3.3-V version and IDT providing both 3.3- and 5-V CPUs (the 5-V version will come out first). The processors also include on-chip power management to minimize active as well as standby power. At 100 MHz, worst-case power consumption is about 4 W, while in its standby mode, the CPU power drain drops to about 30 mW. Management logic dynamically powers down unused circuit sections to reduce power without inflicting any performance penalties.

As mentioned earlier, the Tigershark chip set released by Toshiba in the second quarter of this year can be used with the R4600. This chip set consists of an I/O-controller chip and a cache-controller circuit. The I/O controller basically converts the R4000-family signals to a signal set that makes the CPU and cache subsystem appear to be a 486 local bus. That signal translation then lets the CPU subsystem take advantage of any of the many 80486-motherboard chip sets, which, in turn, can tie the R4000 CPUs into main memory and the EISA or ISA expansion buses.

Because the R4600 processor is software-compatible with the rest of the R4000 family processors, all existing development tools can be used for software development. However, a cache-level simulator—a modified version of the Cache analysis tool from MIPS Technology Inc.—is being developed specifically for the R4600. □

PRICE AND AVAILABILITY

The R4600 processor comes in a 208-lead ceramic quad-sided flat package or a 179-lead pin-grid array. The PGA package is compatible with the R4000/4400PC CPUs, while the 208-lead CQFP provides designers with a new footprint option. Toshiba's CQFP-housed R4600 sells for $250 each in 10,000-unit quantities, with samples available in the second quarter of 1994. IDT will sell its R4600 PGA-housed 5-V version for $240 apiece in 10,000-unit lots, with samples available this month. The Tigershark chip set for NT-compatible platform implementations is available from Toshiba and sells for $65/set in 10,000-set lots. Price for the Mako chip set hasn't been set.

Integrated Device Technology Inc., 2975 Stender Way, Santa Clara, CA 95054-3090; Contact Bob Rowe for embedded or Unix applications and Manual Alba for NT applications, (408) 727-6116. **CIRCLE 519**

Toshiba America Electronic Components Inc., 9775 Toledo Way, Irvine, CA 92718; Jean Claude Toma, (714) 455-2227. **CIRCLE 520**

HOW VALUABLE?	CIRCLE
HIGHLY	541
MODERATELY	542
SLIGHTLY	543

PRODUCTS NEWSLETTER

DSP Design Package Adds Synthesis Tool

The addition of architectural synthesis expands the top-down design capabilities of the DSP Station package from Mentor Graphics Corp., Wilsonville, Ore. DSP Station is an integrated environment that meshes high-level design entry, simulation, analysis, optimization, and implementation for DSP chip and system design. The new synthesis tool, called Mistral2, performs rules-driven architectural synthesis for microcoded digital-signal-processing (DSP) applications. Engineers can use it to create a bit-parallel microcontrolled architecture and its structural implementation, and then automatically generate the microcode to execute the DSP algorithm on the hardware. What-if analysis helps find an optimal datapath architecture. Mistral2 is sold for $100,000 as an option to DSP Station. It runs on HP and Sun workstations. Call (503) 685-7000. *LM* **CIRCLE 710**

Mixed-Signal Simulator Verifies ICs And Boards

A mixed-signal simulator from Dolphin Integration, Meylan, France, helps verify either ASICs or pc boards containing analog and digital circuitry. The simulator, called Smash, employs a native mixed-signal approach in which digital signals are simulated with event-driven techniques, and a single process handles both the simulation and time synchronization between digital and analog portions of the circuit. Smash performs logic simulation using three levels and four strengths. Two different algorithms are available for analog simulation. The first is a direct-method algorithm that's similar to Spice, but with different timestep-control strategy and convergence criteria. The second algorithm is relaxation-based. Smash also includes capabilities for both analog and digital behavioral modeling. The Smash simulator runs on PCs, Macintosh computers, and Unix workstations. Call (33) 76411096 for pricing and additional information. *LM* **CIRCLE 711**

Windows Tool Eases Multimedia Creation

At some point in a development cycle it's time to make a presentation to management or customers to describe the project, results, or capabilities. Though presentation software packages that create foils and slides are readily available, such media is commonplace and may not generate the enthusiasm that belies the information being conveyed. Enter Super Show and Tell, a multimedia presentation-development package from Ask Me Multimedia Center, Minneapolis, that runs under Microsoft Windows 3.1. SST allows users to create interactive multimedia presentations in a free-form enviroment that uses a slide-carousel as a metaphore and can include sound and motion without using a complex authoring language. The software can crate colorful charts, import still-frame pictures, annote the illustrations with sound, or create animated sequences. The opening screen includes a 1/4 screen preview window, five thumbnail slides, a set of VCR-like control buttons, and a set of positioning controls for alignment and centering. Modeless editing allows users to smoothly switch among five different media editors without leaving the original screen. The software also includes context-sensitive help in all modes. The software requires an 80386SX or newer system with a minimum of 2 Mbytes of RAM and a VGA display and mouse. SST sells for $149, including free technical support. *DB* **CIRCLE 712**

Digital Sensor Yields Accurate Temperatures

With the ability to provide direct digital temperature readings in less than 1 sec. with no external devices, an all-digital sensor provides better accuracy than mixed sensor/a-d converter combinations for low-cost systems. The sensor chip, developed by Dallas Semiconductor, Dallas, Texas, is fully-calibrated at the factory and can resolve temperatures to within 0.5 °C over a -55 to +125 °C range. Accuracy is maintained to within 0.5 °C over a 0 to 70 °C range. To perform the temperature-to-digital conversion, the DS1620 sensor employs two oscillators, with each oscillator's frequency determined by resistors with different temperature characteristics. The resistor values are calibrated at the factory, providing users with a simple solution that shortens the development cycle by removing the need to calibrate at the system design stage. The sensor can function as a standalone thermostat, with predetermined set point stored in nonvolatile memory, and can activate heating and cooling devices. By integrating all the conversion and the sensor on the same chip, all the potential analog noise that could be picked up by wires, which would otherwise connect a sensor to an a-d converter, can be eliminated. *DB* **CIRCLE 713**

Edited by Clifford Meth

Enhanced Standard Cell Family Targets 3-V Supply Systems

An upgrade to its sub-micron CMOS process that optimizes it for 3-V operation makes it possible for NEC to provide an enhanced 0.5-μm standard-cell family. That family can be used to create custom designs of up to 600,000 gates, including blocks of ROM and static RAM. The CB-C8 standard-cell family supplements NEC's CMOS 8L and LCX families of 0.5-μm gate arrays. The high-density chips are made possible thanks to the low power consumed by each gate—about 0.8 μW/gate/MHz—approximately one-third that of the company's CB-C7 family.

Internal toggle frequencies of the flip-flops go up to 175 MHz, while an unloaded two-input NAND gate (fanout of 1 with no metal load on the output) exhibits a propagation delay of just 130 ps. Such high speeds suit the library for use in high-performance workstations, communication systems, and many other applications. Available megafunctions include NEC's V30MX core, an 8086-compatible CPU that can operate at up to 33 MHz; 8237A DMA controllers; PLLs to synchronize on-chip timing; and many other blocks. Megacells are supported by Verilog gate models to ease chip simulation. The library can be installed on most design platforms.

On-chip SRAM can be added in blocks as large as 64 kbits each (synchronous or asynchronous), or ROM in blocks of 256 kbits. Bus interface options include GTL (Gunning transceiver logic) for fast, low-noise transfers, and for systems not ready for 3-V operation, I/O cells in the library provide interfaces to 5-V systems. Also expected by the first half of 1994 are RAMbus interface cores, and a-d and d-a converters. Pad rings with up to 440 I/O pads are now available, with double that number by late 1994. An example design in a 208-lead PQFP that uses the V30MX CPU core, 20,000 gates, and 64 kbits of RAM sells for about $50 each in lots of 10,000 units/month.

***NEC Electronics Inc.**, 475 Ellis Street, P.O. Box 7241, Mountain View, CA 94039-7241; Kazuhiro Endo, (415) 965-6000.* CIRCLE 601

■ *DAVE BURSKY*

Speedy Graphics Controllers Tie To PCI And VL Buses

A trio of graphics controllers, two targeted for DRAM-based graphics subsystems and one for VRAM-based systems, deliver performance levels from about 24 million up to about 50 million Winmarks. The first two controllers provide single-chip system upgrades for the existing CL-GD542x and 543x families; the third offering, a two-chip, starts a new high-end 545x family. The chips also comply with the VESA-defined monitor signalling standard for "Green" PCs.

The CL-GD5429 fills out the high end of the 542x family and offers a 20% to 30% speed boost over the already available 5428, while maintaining a pin-compatible footprint, thus easing system upgrades. At the low-end of the 543x family, the 5430 is a pin-compatible, slightly lower-performance version for cost-sensitive systems. Tackling higher-performance needs, the 5452/5453 chip set employs high-speed VRAMs to obtain the bandwidth needed to provide 50 million Winmarks and true-color high-resolution images.

The CL-GD5429, a memory-mapped I/O VGA controller, has extensions to accelerate some GUI functions, delivering up to about 25 million Winmarks. It supports true-color with 640-by-480 or 800-by-600 pixels, 16-bit color at 1024-by-768 pixels, and 8-bit color with 1280-by-1024-pixel resolution. It includes ISA and VL-bus interfaces and runs at dot-clock rates of up to 86 MHz. Integrated into the 160-pin circuit is a 24-bit RAMDAC and a dual frequency synthesizer, minimizing component count. Offering a similar level of integration, the 5430 also includes the synthesizer and RAMDAC but comes in a 208-lead package. The chip forsakes the 16-bit ISA-bus interface and instead packs a 32-bit PCI-bus interface along with the VL-bus option. For the fastest PC graphics, the CL-GD5452/5453 chip set delivers up to 50 million Winmarks and displays true-color images with up to 1280 by 1024 pixels, or up to 256-color images with 1600 by 1200 pixels. The GD5452 controller has a 32-bit VL/PCI/ISA host-bus interface (user selectable), a 64-bit video-memory interface that can address up to 4 Mbytes of VRAM, and an on-chip 64-bit acceleration engine with stylized X,Y line-draw capability. The supporting GD5453 palette d-a converter has a 128-bit-wide interface to the video memory and delivers dot clocks at up to 135 MHz.

Both chips come in 208-lead PQFPs. Samples are available now. In lots of 1000, the GD5429, 5430, and 5452/5453 sell for $27, $30, and $65 each, respectively.

***Cirrus Logic**, 3100 W. Warren Ave., Fremont, CA 94538; Tom Kao, (510) 226-2272.* CIRCLE 602

■ *DAVE BURSKY*

Futurebus+ Interface Supplies Cache Control

The CC89602 multi-profile 64-bit Futurebus+ interface chip contains an integrated cache controller to support tightly-coupled multiprocessing. In addition, the part offers full CSR support for Futurebus+ profiles A, B, M (military), and T (telecomm). There's also an on-chip distributed- and central-arbitration controller built in. A bidirectional FIFO buffer adds support for compelled-mode transfers and targeted interrupts, while the chip can handle a data-transfer rate of 160 Mbytes/s. Samples of the CC89602 are available now. In small quantities, it will sell for just over $300. RN

Cable & Computer Technology Inc., 1555 South Sinclair St., Anaheim, CA 92806; (714) 937-1341. CIRCLE 603

RAMDAC'S 24-BIT PORT SPEEDS DATA TRANSFERS

By widening the interface port to 24 bits on its highly-integrated video DAC, designers at Oak technology can double or triple the data transfer rate between the graphics controller and the RAMDAC. The higher transfer rate allows the implementation of 16- or 24-bit color displays (up to 16 million colors) without increasing the system clock frequency. The OTI-088 also integrates the clock generation circuits, eliminating the need for multiple external oscillators.

The 24-bit pixel interface port makes it possible for a companion graphics controller to load 8-, 16-, or 24-bit data in a single bus transfer cycle. Most other high-integration RAMDACs have only an 8-bit pixel port, thus requiring two or three bus cycles to transfer 16- or 24-bit color images.

In addition to the 24-bit mode, the chip supports 64k-, 32k-, 256-, or 16-color display modes. Moreover, in addition to loading the parallel pixel data faster, the chip can also deliver RGB (red-green-blue) pixel streams at data rates of up to 135 MHz. Such high data rates allow the chip to deliver 1280-by-1024-pixel images at refresh rates of up to 75-Hz, non-interlaced—most other inexpensive RAMDACs have top rates of about 80 Mpixels/s.

The internal clock oscillator employs an external 14.318 MHz crystal that is multiplied by two phase-locked loops, one generating a clock for the video memory and the other the master clock for the graphics controller. Also included in the OTI-088 is a power-down mode that helps extend PC notebook battery life when the chip drives external RGB displays, or trims power in "green" PC systems. The mode drops the active current of 120 mA to a standby level of 20 mA.

The chip comes in an 80-lead PQFP and sells for $10 each in quantities of 1000. An 84-lead PLCC package is also available as an option. Samples are immediately available.

Oak Technology Inc., 139 Kifer Court, Sunnyvale, CA 94086; Scott Alberts, (408) 737-0888. CIRCLE 604

■ *DAVE BURSKY*

DRAM CONTROLLER RUNS TOP-PERFORMING DRAMS

With the ability to operate at system clock speeds of 40 MHz, the DP8440 and 8441 DRAM controllers make it possible for designers to implement very-high-performance memory subsystems. The DP8440 supports DRAMs with capacities of up to 16 Mbits and data paths of 8, 16, or 32 bits, while the DP8441 can control up to 64-Mbit DRAMs with data paths as wide as 64 bits.

The programmable chips support a wide variety of CPUs—the Intel i860, 486, and 386, as well as Motorola's 68030 and 68040 and National Semiconductor's NS32GX320, 32SF640, and the MIPS R3000 and 4000 RISC chips. The controllers can handle the automatic microprocessor burst mode accesses and support fast page mode, static column mode, and nibble-mode DRAM configurations. On-chip phase-locked loops form part of a precision delay line that generates the sub-clock delays to ensure precise system timing. Both chips include high-drive output buffers, eliminating off-chip drivers for memory arrays of up to 256 Mbytes using 16-Mbit DRAMs and up to 512 Mbytes when 64-Mbit DRAMs are available.

The DP8440 comes in an 84-lead PLCC and sells for $43.06 each in lots of 1000; the 8441 comes in a 100-lead PQFP and sells for $49.04 each in similar quantities. Both are available now. DB

National Semiconductor Corp., P.O. Box 58090, M/S 16300, Santa Clara, CA 95052-8090; (408) 721-5000. CIRCLE 605

ERROR-CORRECTION IC FAMILY IMPROVES DRIVE PERFORMANCE

A family of hard-disk drive controllers features advanced data integrity and error-correction code (ECC) technology. Using the parts, drive makers can implement the synchronous read-write channels, advanced servo controllers, and thin-film and magneto-resistive heads to maximize storage densities. The chips' data-integrity features include on-the-fly header identification error correction; programmable, multiple-burst, on-the-fly field error correction; and block cyclic redundancy check.

The family is designed to handle the three most popular drive interfaces: the CL-SH5600 works with the IDE format; the SH5700 is intended for SCSI applications; the SH385 is designed for PCMCIA-based drives. The IDE and SCSI chips employ data-streaming techniques that allow the host processor and disk to transfer data in an automated fashion to prevent buffer under- and over-run. This increases the drive's data-transfer rate by reducing the processor's overhead.

The SH385 combines the ECC features with an advanced Winchester formatter, a dual-port memory manager, and a complete host interface for drives compatible with the PCMCIA ATA standard. The part can handle data rates up to 44 Mbits/s at 5 V, and 40 Mbits/s at 3.3 V.

The SH5600 and SH5700 are housed in 100-pin plastic quad flat packs and very small quad flat packs (VQFP). Samples of both parts will be available in the first quarter of next year. In quantities of 1000, the SH5600 costs $20 and the SH5700 sells for $22. The SH385 fits in a 120-pin VQFP. It sells for $20 in lots of 1000, and samples are available now.

Cirrus Logic Inc., *3100 West Warren Ave., Fremont, CA 94538; (510) 623-8300.* CIRCLE 606

■ *RICHARD NASS*

TRANSFER DATA FROM A PORTABLE TO A DESKTOP WITH NO WIRES

One of the problems associated with PCMCIA-based portable computers is that there's no easy way to transfer data between the system and another system. Most of the portables aren't built with floppy drives to save power, size, and weight. So the most popular method was to connect the two systems using a cable between the serial or parallel ports and running a file-transfer utility. Now, thanks to an infrared wireless adapter from IBM, users can throw those cables away.

The adapter comes in two pieces, one for the PCMCIA-based portable and one for the ISA- or MCA-based system. The card consumes about 250 mW in the portable. A line-of-sight connection isn't necessary. The two systems just have to be in the same room (about 30- by 30-ft. room). The non-compressed data transfer rate is 1 Mbit/s. The units are available now. The ISA- and MCA-based components cost $499, while the PCMCIA side sells for $599.

***IBM Technology Products**, P.O. Box 100, Somers, NY 10589; (914) 766-1900.* **CIRCLE 607**

■ *RICHARD NASS*

LOW-COST X-TERMINALS PUSH 150,000 X-STONES

X-terminal users can get up to 150,000 X-stones from the XP350 series displays. The XP350 units are built with a 33-MHz Mips R3000 processor, which has an integrated graphics processor for high-speed windowing. Three models are available: the XP354 19-in. terminal with

256 gray scales and 1280-by-1024-pixel resolution; the XP356 17-in. color display with 1280-by-1024-pixel resolution; and the XP358 19-in. color display with 1280-by-1024-pixel resolution. Front-panel controls let users adjust brightness, contrast, image size, and RGB intensities. Available now, prices for the XP350 family range from $2495 to $5495. RN

Tektronix Inc., 26600 S.W. Parkway, P.O. Box 1000, Wilsonville, OR 97070. **CIRCLE 608**

DIGITAL ANALYZER HAS X WINDOWS INTERFACE, NETWORK CAPABILITY

With full networking capability and X Windows compatibility, the Enterprise DAS (digital analysis system) allows designers to integrate systems analysis with other electronic design automation tools. The result is more effective verification and debug of complex real-time systems, particularly those based on multiple or high-end microprocessors.

Built-in 92XTERM software permits software engineers to access the Enterprise DAS from any X Windows system, so users can work in their familiar environment and share resources with other team members. Also, users can integrate data from other X Windows software. Those who want the X Windows interface but don't need to share a system among many workstations can buy a stand-alone version.

Software and hardware engineers and system integrators can work with their high-level debugger in one window and see the same code in a real-time trace in another window. Through the LA-Connect program, which extracts symbolic information from third-party compilers and reformats it for the Enterprise DAS, integrators can set sophisticated hardware breakpoints and trace their code in real-time.

The XTERM software is warranted fully compatible with the Sun Sparcstation. It is also compatible with the X11/R4 release of X Windows and has been demonstrated on multiple platforms

A fully configured Enterprise DAS starts at $33,000. Stand-alone systems start at $30,000.

Tektronix Inc. *Test and Measurement Group, P. O. Box 1520, Pittsfield, MA 01202; (800) 426-2200.* CIRCLE 609

■ *JOHN NOVELLINO*

FAST DIGITAL IC PRODUCTION TESTER IS ALSO ECONOMICAL

Aimed at digital IC production test, the HP 83000 F330t offers high performance and faster test setup, while reducing purchase price and operating costs. The system allows at-speed testing to 330 MHz, with an overall timing accuracy of ±300 ps.

The tester uses a new waveform generation technique called "change-waveform-on-the-fly" to permit greater timing flexibility than return-to-zero and non-return-to-zero formats and the conventional "change-timing-on-the-fly" technique. Users can create complex, applications-oriented timing waveforms in accordance with the device-under-test's data sheet. High throughput is provided by a test-per-pin architecture, which includes a test processor and memory for each pin; a fast workstation with a fiber-optic data transfer link; and a "throughput optimizer" in the system software. Scan and I_{DDQ} options are available.

The HP 83000 F330t software suite provides a unified engineering and production test environment, with fast design-to-test links and short set-up and debug times. A specially designed testhead manipulator ensures smooth docking to other equipment. The system's modular construction, high level of integration, and liquid cooling offer a compact, reliable design that is easy to repair. Modularity also allows for future expansion and upgrades. The system will initially come with up to 512 I/O channels, with 1024 channels available in the future.

The HP 83000 F330t can be ordered now, with first shipments in June 1994. A typical 256-channel system will cost about $1.5 million.

Hewlett-Packard Co., *Direct Marketing Organization, P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844.* CIRCLE 610

■ *JOHN NOVELLINO*

TEST SOFTWARE DELIVERS HIGH FAULT COVERAGE

An automated IC test-creation system, called ATTDFT for IC Design, uses a patented constructive partial-scan capability to ensure high fault coverage with minimal chip area devoted to testability. The circuit control and observability supplied by the system allows changes to be made to the testability structure in real time.

ATTDFT for IC Design permits sequential test generation, which allows users to create test patterns to detect faults in a broad range of circuit types. Other technologies employed include I_{DDQ} testing for accurate observation of every node in a circuit, time-constraints analysis for determining a circuit's critical areas, and partial-scan synthesis, which increases testability in synthesized designs. The system accepts either synthesized or manual designs.

The constructive partial-scan tool performs a static timing analysis using the propagation delay of scan flip-flops in the target library. Flip-flops on paths that do not meet timing specifications are not scanned. The names of these flip-flips are fed into the constructive partial-scan selection tool. Testability tools that use a deselection or destructive approach to flip-flop selection will scan all flip-flops except those on the no-touch list. The ATTDFT partial-scan approach directly finds the flip-flops that when scanned will make the chip testable. Typically, this technique offers high fault coverage with 30% to 40% of the flip-flops scanned, compared to 80% to 90% for deselection techniques.

The company plans to package other technologies into the system as part of a strategy to deliver a unified device test-creation package. Included will be boundary-scan insertion capability (in the first half of 1994), with a descriptive language editor that will determine the legality of boundary-scan definitions and register insertions. Later in 1994 the system will offer low-overhead testability for random-logic design using random-logic built-in self-test (BIST). In 1995, BIST for structures such as RAM and ROM will be added.

ATTDFT, which runs on HP and Sun platforms, will be available in the first quarter of 1994. A per CPU license price of $110,000 supports multiple users on a Sparc 10 Station. A Mentor Integration package costs $10,000.

AT&T Design Automation, *Crawfords Corner Rd., Holmdel, NJ 07733; (908) 949-3000.* CIRCLE 611

■ *JOHN NOVELLINO*

GENERATOR LINE HANDLES RANGE OF APPLICATIONS

A line of 10 high-precision waveform generators spans a wide range of test and measurement applications. The line includes functions generators, arbitrary function generators, arbitrary waveform generators, and a pulse generator.

Two low-cost function generators feature a 10-MHz maximum frequency. The 2310 costs $695, and the 2311, which includes sweep and modulation capabilities, costs $995. Two other function generators are fully IEEE-488 programmable. The 10-MHz 2410 costs $1695, and the 20-MHz 2420, which works to 20 MHz and has a 15-V pk-pk output and a burst mode, is $2795.

The line includes three arbitrary function generators that combine arbitrary waveform and standard waveform generation capabilities. The 2411 and 2414 are 10-MHz, 10-V pk-pk units with burst, sweep, and modulation functions. Both have 12-bit resolution. The 2411 ($1995) has a 1-Msample/second sample rate and 8-ksample storage. The 2414 ($2495) has a 10-Msample/second sample rate and 16-ksample storage.

A pair of arbitrary waveform generators are fully compatible with IEEE-488 and the standard commands for programmable instruments (SCPI). Both units have 12-bit resolution and minimum 32-ksample memories. The 2605 ($1995) has a 10-Msample/second sample rate. The 2620 ($3495) has a 25-Msample/second sample rate and a maximum memory of 128 ksamples.

The pulse generator, the 2550, is designed for comparator and device testing, telecommunications, and ATE applications. The instrument's maximum frequency is 50 MHz, with a 10-V pk-pk output. It features a burst mode and variable symmetry. Delay, width, polarity, amplitude, offset, and rise and fall times can be varied. The 2550 costs $4995. Delivery times for all units are four to six weeks after receipt of an order.

Analogic Corp., *8 Centennial Dr., Peabody, MA 01960; (508) 977-3000.* CIRCLE 612

■ *JOHN NOVELLINO*

SOFTWARE LINKS TEST INSTRUMENTS AND PCS

The HP 34800-series BenchLink Software allows users to send data between HP Basic Test Instruments and personal computers without the need for programming. The Windows-based packages feature an easy-to-use intuitive user interface and point-and-click operation. The BenchLink/Scope package captures screen images and waveform data from HP 54500- and 54600-series scopes for transfer to other Windows-based programs for analysis or presentation. The BenchLink/Arb package allows users to create standard and arbitrary waveforms and send them to an HP 33120A function/arbitrary waveform generator for output. Arbitrary waveforms can be generated using a freehand drawing palette or by editing standard or captured waveforms. BenchLink/Scope costs $249, and BenchLink/Arb costs $295. JN

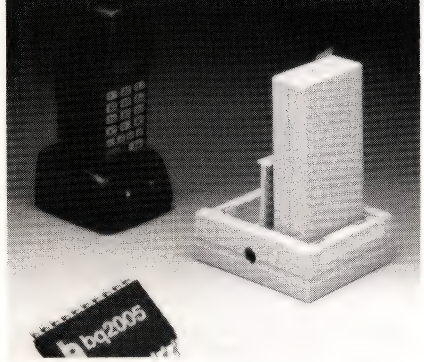
Hewlett-Packard Co., Direct Marketing Organization, P. O. Box 58059, MS51L-SJ, Santa Clara, CA 95051-8059; (800) 452-4844.

CIRCLE 613

IC Controls Charging Of Two Separate NiCd/NiMH Batteries

Benchmarq has come up with a single charge-control IC that independently controls the charging rate of two completely separate nickel Cadmium (NiCd) or Nickel Metal Hydride (NiMH) secondary batteries. The bq2005 provides a cost-effective means to quickly and safely fast-charge two independent battery packs. In addition, it can be used as a frequency-modulated controller at speeds to 300 kHz for switchmode regulation of the charging current. It may also be used with a linear regulator or transistor to gate an external dc current source.

Because the bq2005 supports both NiCd and NiMH batteries, it allows charger upgrades from designs for NiCd batteries to NiMH battery technology without a redesign. It supports charge rates of 1 to 1.5 hours to NiMH, and as quick as 10 to 20 minutes for the appropriate NiCd batteries. The fast-charge mode begins with the application of the charging supply or by replacement of the battery. For safety, charge is inhibited until the battery temperature and voltage are within specified limits. Battery temperature, voltage, and time are monitored throughout fast charge. The chip's charging algorithm includes a "top off" charge at 1/8 the charge rate for NiMH batteries, as well as a user-selectable pulsed trickle charge rate



of C/32 or C/64.

To determine when to terminate charge, the bq2005 calculates the slope of the battery temperature rise curve ($\Delta T/\Delta t$). It uses the rapid temperature increase associated with fully charged batteries to terminate fast charging when the rate of temperature increase exceeds a predetermined limit. The criteria $\Delta T/\Delta t$ is backed up by detecting when the battery voltage starts to drop, so called negative delta V ($-\Delta V$). For true fail-safe termination, fast charging for longer than a preset time terminates operation. The bq2005 comes in 20-pin DIPs and SOICs. In lots of 1000, the DIP costs \$4.70 each; the SOIC is \$4.80 each.

***Benchmarq Microelectronics, Inc.**, 2611 Westgrove Drive, Suite 109, Carrollton, TX 75006; David Heacock, (214) 407-0011.* CIRCLE 614

■ *FRANK GOODENOUGH*

P-Type MOS FETs On A Chip Source

Not everyone needs 64, 375-V, open-drain 500-μA p-channel MOSFETs on one chip. But applications for the Supertex HV49 range from non-impact printers and plotters to ATE systems. In a 80-pin flatpack, the HV49 employs a serial I/O for data. It can be considered a cascadable serial-to-parallel converter with a clock rate exceeding 6 MHz. The 5-V CMOS logic includes latch- and output-enable functions, and drift direction. The HV49 is built on a Supertex HVCMOS II process, combining high-speed, low-power CMOS logic on a chip with high-voltage CMOS. Used to form half or full bridges with the company's HV31, its n-channel counterpart allows multiple complementary high-voltage bridges, which can be driven easily from 5-V logic without special high-side-switch drive circuits. The HV49 is specified for operation over the commercial temperature operating range. In lots of 1000, it costs \$10.39 each.

***Supertex**, 1350 Bordeaux Dr., Sunnyvale, CA 94089; Dillip Kapur, (408) 734-5247.* CIRCLE 615

■ *FRANK GOODENOUGH*

INTERACTIVE SPICE SIMULATION ENVIRONMENT DISPLAYS CIRCUIT WAVEFORM DATA IN REAL TIME

An interactive Spice simulation environment from Intusoft lets users change circuit component values and watch the resulting performance changes in real time. The ICAP/4NT and ICAP/4Macintosh systems consist of schematic entry, the company's interactive IsSpice4 simulator, model libraries, and graphical waveform analysis. With the ICAP system, designers can simulate almost any analog or mixed-signal circuit, including RF, power, ASIC, and filter designs.

Users may employ their own schematic entry system, or take advantage of the company's SpiceNet integrated entry software. ICAP directly accepts Spice net lists produced by most schematic vendors. However, users can drive the entire simulation process with the integrated SpiceNet, including circuit editing.

The IsSpice4 simulator is an interactive version of Spice. Once the simulation starts, users are free to explore the design by running analyses, changing circuit values, and measuring performance. Simulation runs can be started, stopped, stepped, resumed, or aborted at any time. And when the simulation is running, waveforms for any circuit point can be displayed in real time. IsSpice4 can access voltages, currents, device power dissipations, and a wide range of computed device parameters, such as transconductance.

Over 5000 models are included with the ICAP system, many of which aren't available from other Spice vendors. In addition, extra modeling options include an RF device library and the company's SpiceMod program that creates models from datasheet values.

ICAP/4NT runs on 80486-, Pentium-, or Alpha-based machines running Windows NT. ICAP/4Macintosh runs on computers running Macintosh Systems 7.x. Both versions are shipping now for $2595.

***Intusoft**, P.O. Box 710, San Pedro, CA 90733-0710; (310) 833-0710.* **CIRCLE 616**

■ *LISA MALINIAK*

FPGA FITTER PROVIDES PATH FOR PAL USERS

The ACTmap FPGA Fitter from Actel provides an upward-migration path for engineers currently using PAL devices. ACTmap is an optimization tool that efficiently integrates multiple PAL devices into one Actel FPGA. It accepts designs in Palasm format, or as EDIF net lists. Then, it maps the logic into an Actel architecture. ACTmap is included with the company's Designer series development systems that run on PCs and Unix workstations. The Designer development system, which supports Actel devices with up to 2500 gates, costs $995. LM

Actel Corp., 955 E. Arques Ave., Sunnyvale, CA 94086; (408) 739-1010. **CIRCLE 617**

SPICE SIMULATOR RUNS IN FREQUENCY DOMAIN

Super-Spice is an RF, microwave, and high-speed time- and frequency-domain simulator that overcomes many limitations of simulators that run only in the time domain. It's based on a C-language version of Berkeley Spice, but adds frequency-domain conversion enhancements. With Super-Spice, engineers can use frequency-domain techniques to predict potential problems in high-speed, high-density digital circuits. In addition, the schematic-driven simulator has accurate models of single and multiple-coupled lines, transmission media, discontinuities, and loss. An electromagnetic module allows users to analyze multi-layer media, and the resultant parameters can be used in subsequent simulations. Super-Spice is part of a complete suite of high-frequency tools. It runs on Unix workstations. Call the company for pricing. LM

Compact Software Inc., 201 McLean Blvd., Paterson, NJ 07504; (201) 881-1200. **CIRCLE 618**

DFA TOOL ENSURES THAT PC BOARDS CAN BE BUILT

ATTDFA is a design-for-assembly package that includes a suite of audits and checks to ensure that pc-board designs adhere to assembly guidelines. The software is completely design-rule driven, which provides users with control and flexibility. Rules cover both general and specific instances, and are contained in libraries that can be tailored for projects, manufacturers, and product lines. All of the audits generate hard-copy reports, and also support graphical display for fast and easy cleanup of assembly violations. ATTDFA will be available early next year. It runs on HP and Sun workstations, and costs $15,000 per floating license. LM

AT&T Design Automation, Crawfords Corner Rd., Holmdel, NJ 07733; (908) 949-3000. **CIRCLE 619**

VERILOG-HDL DEBUGGER ADDS 2D CAPABILITY

The Magellan graphical debugging environment for Verilog HDL simulators now has 2D capability. Two-dimensional debugging means that users can fix their designs by tracking values while moving forward or backwards in time or space, without having to re-simulate the design. Using simple point-and-click operations, users can find the cause of a problem by stepping through the time cycles and the topology of a circuit while viewing the corresponding values and waveforms. Magellan runs on HP and Sun workstations. It's shipping now, with licenses starting at $1995. Free evaluation licenses are also available. LM

Systems Science Inc., 1860 Embarcadero Rd., Suite 260, Palo Alto, CA 94303; (415) 812-1800. **CIRCLE 620**

Physical Design Software Helps Build Advanced Megagate ASICs And Large Structured-Custom ICs

Two new physical-design products from Cadence help engineers build megagate ASICs and multimillion-transistor ICs. The first of the two products, Gate Ensemble 4.3, is a place-and-route system that comes with a crosstalk-intelligent ASIC router, vendor-independent embedded-block design capabilities, and a new high-speed placement engine. The second product, Chip Assembly Solution, is a top-down, timing-driven environment for creating structured-custom ICs.

Gate Ensemble is tailored for 0.5-micron ASIC technology, which is sensitive to second-order effects. The tool's crosstalk router automatically identifies potentially hazardous nets, manages routing tracks to eliminate crosstalk, and then reviews and incrementally reroutes portions of the design to eliminate any new crosstalk sensitivities.

The Embedded Block Design System (EBDS) is a Gate Ensemble option that simplifies block creation while supporting vendor independence. Another option is the Tzeng router, which is a new quadratic placement engine that combines the speed of channel routing with the versatility of maze routing.

Chip Assembly Solution is a top-down environment tuned for multimillion-transistor processor designs with strict performance requirements. The timing-driven design flow spans across the system's floorplanning, standard-cell, and complex-block design capabilities. These timing features, which include block-timing budgeting and multilayer timing-driven place and route, can improve clock speed by up to 25%.

Other key Chip Assembly features include automatic ECO support throughout the design flow, and an open block-import format that allows for reuse of blocks created with Cadence or third-party layout tools. Also available are specialty routers optimized for microprocessor design, such as a flexible bus router.

The Gate Ensemble modules will ship by the end of the year, with pricing starting at $50,000 each. Chip Assembly Solution, also shipping by year's end, starts at $216,000. All the software runs on workstations.

Cadence Design Systems Inc., 555 River Oaks Pkwy., San Jose, CA 95134; (408) 943-1234. CIRCLE 621

■ LISA MALINIAK

JUST HIGH SCHOOL AND OHM'S LAW

For some months, now, I have taken an interest in your musings concerning the plight of EEs in the job market and with the relevant educational structure involved. I, among many, was initially distraught at the nature of the work and curricula required for a BSEE, with all the seemingly irrelevant and theoretical contortions of idealistic mathematics, and the petty lab exercises with its excruciating protocol in reporting the results. It is no wonder that so much of the school experience is reduced to the level of survival at all costs, incorporating slick ways to copy old reports and tests, using prewritten computer code for projects, and whatever else might lighten the burden to endure the perceived nonsense of the classroom.

Ultimately, however, I began to see the beauty of the physics and actually got excited about the world of theoretical descriptions and potentialities within our trade. However, at about this time of budding enthusiasm came a major disorientation—the onset of job interviews, meager though they were. It seems that while employers were universally on the prowl for stellar academic performers, they offered no commensurate opportunity within their organizations. The engineering jobs were extremely fraught with administrative burdens of purchasing, costing of outside services, record keeping, and providing services to internal customers who knew nothing of the world of technology. Nobody seemed to want hardware designers or people to remain on the cutting edge of specific technologies. In fact, most interviewers were totally uninterested in the content of the curriculum, but just wanted to know about my grades, people and communication skills, and programming languages mastered. They actually admitted that an engineering education is viewed as a boot camp, a filter of people, and not of much value in and of itself.

From the past three years of watching the job postings at the university career centers, this recurring situation has left me to conclude it is the rare advanced degreed workaholic, more often than not of foreign extraction, who can continue the excitement of the classroom into the design world. The rest of us are left to allow our memories of p-n junctions and state diagrams to fade back into childhood ignorance as we scramble to make our mundane tasks seem like an expert is required just to preserve whatever foothold on a job we may have. The IEEE is as useless and irrelevant as ever, rubbing my nose into its academic world of quasi-reality, and the same goes for any

1967-1993: WHAT'S CHANGED?

I read your Sept. 2 issue Editorial about your musings while traveling I-80. I lived in New Jersey for almost 30 years and I too have had occasion for similar musings on that road. Because of the radical changes and downsizing that has occurred in the world of engineering, I am now musing on Route 128 in Massachusetts.

You ask about the long term outlook for employment of EEs. EEs never really had long-term possibilities for employment unless you were one of the lucky ones, as I was. As evidence of this, I submit a copy of an editorial that ran in your magazine in 1967 [Electronic Design, April 12, 1967, p. 51 (see reprint, left)] entitled "Life Begins At Forty...Will It For You?" It quotes from an impressive study that indicates that regardless of one's credentials and accomplishments, our industry considers an engineer over forty as ready for the dung heap.

Until engineers wake up and demand that their technical societies protect their interests as the AMA does for doctors, then we will continue to have dismal long-term employment prospects.

IRWIN COHEN
CONCORD, MASS.

The Editorial, written by Electronic Design Technical Editor Pete Budzilovich, seems to carry even more weight today, 26 years later.—Ed.

EDITORIAL

Life begins at 40 . . . . Will it for you?

Countless words have been written and spoken about whether engineers should be considered professionals alongside physicians, lawyers and the like. Every kind of parallel has been drawn; the dissimilarities have been pointed up. One factor merits particular attention, yet is too often shunned in discussion—the age obsolescence of engineers.

Where doctors and lawyers are concerned, for instance, a man only gains in value as he accumulates experience, and this increases only with age. In fact, a 45-year-old doctor is deemed a relatively young man.

What about engineers? A recently published report* is packed with data supporting the view that an engineer 45 years of age or older faces a grim future in terms of his possibilities of employment. It indicates, moreover, that no amount of professional training can change this. Thus (and we quote): "Irrespective of their [engineers'] educational background, pre-layoff salary, technical publications, patents, readership in technical magazines, and membership in professional societies, older engineers and scientists remained unemployed for much longer periods of time" [than younger men].

This, coupled with the fact that the huge postwar generation of engineers is rapidly approaching its forties, is frightening.

What is the solution? Obviously the first step is to look into the causes of the situation. What is behind it? Is it the high pay? Or is it the influence of life and medical insurance companies? Whatever it is, the time to find out all about it and take steps toward a satisfactory solution is running out.

Furthermore, in view of the fact that the existing engineering societies do not seem to be concerned with the welfare of their members, concrete steps toward creation of a new organization to study and remedy the problem seem in order.

So next time you talk about professional status, bear in mind the simple truth that you may well be forced into retirement at about 45, unless you migrate into the ranks of management and, as usually is the case, desert the profession per se.

PETER N. BUDZILOVICH

*R. P. Loomba, *A Study of the Re-employment and Unemployment Experiences of Scientists and Engineers Laid Off from 62 Aerospace and Electronics Firms in the San Francisco Bay Area during 1963-65* (San Jose, Calif.: Manpower Research Group, Center for Interdisciplinary Studies, San Jose State College, 1967).

form of professional certification.

If engineering school is seen as nothing but an obstacle course by both the student and the company, as it well is, then why not just let the student major in physics—art for art's sake if you will. At least then you might drive a taxi and still feel good about it. For now, I can do anything in my industry with a good high school education and a course in Ohm's Law. If anything is to be done to stem the trend of disillusionment within the engineering profession, it has got to come with a realistic assessment of the nature of the real world of companies' needs and what requires the skill of an engineer in the first place. Meanwhile, all my bizschool, party-hearty buddies are laughing all the way to the bank.

WILLIAM B. FARRIS
ALABAMA POWER COMPANY
BIRMINGHAM, ALA.

THE REAL STORY ON THE LIFEBOAT RADIO

In the Sept. 2 issue, the "40 Years Ago in Electronic Design" column contained an item on a 56-lb. lifeboat radio, developed by Mackay Radio and Telegraph Co., New York, N.Y., that automatically transmitted SOS signals. At the end of the item, we questioned whether the 56 lbs. included the batteries.

We received a telephone call from Thomas E. Smith, director of government programs for the company, now Mackay Communications Inc., Edison, N.J. (today they make shipboard satellite receivers for the Navy). Smith informed us that the Mackay Model 401 lifeboat radio had no batteries, but was powered by a hand-cranked generator. The unit was buoyant and was designed to be thrown overboard from the ship during an emergency and retrieved by people in the lifeboat.

Below are Smith's follow-up letter to our telephone conversation, and two letters from readers who had personal experiences dealing with this radio:—Ed

A HEARTY FILAMENT REQUIREMENT

Mackay Communications Inc., formerly the Marine Division of Mackay Radio and Telegraph, is proud to see one of our older products remembered in Electronic Design. The article describes our model 401A lifeboat radio designed for use by Merchant seamen in a lifeboat during a distress at sea.

In the mid-seventies, the radio was redesigned and made lighter, 38 lbs. A smaller motor-alternator was driven by the hand cranks. This could be achieved because the 401A used vacuum tubes with a hearty filament requirement and the 403A is completely solid state. All other capabilities remained the same.

The 403A radio is still in use today, but with the Global Maritime Distress and Safety System (GMDSS) now being implemented, it will no longer be required.

THOMAS E. SMITH
MACKAY COMMUNICATIONS
EDISON, NJ

IT WAS THE GIBSON GIRL...

At the end of the item on the lifeboat radio, the editor added (looking for a little humor): "Did that 56 lbs. include the batteries? We wonder."

In fact, the truth is: It didn't have any batteries! This is the famous "Gibson Girl" lifeboat radio and it was powered by a crank generator. It was packaged in a die-cast waterproof aluminum case, about 20 × 12 × 12 in. with an unusual shape. The two sides were concave surfaces and the unit was gripped between your knees while sitting in a lifeboat (rubber raft). It was not transistorized; the oscillator/output stage was a tube (now called "a fire FET").

The crank drove the generator rotor and a mechanical sequencing device that keyed "SOS" a few times, sent a continuous carrier (for direction finding), and then changed to the alternate emergency frequency. The unit had a small light that came on to indicate when the generator was spinning fast enough. Believe me, keeping that generator going for more than a minute or two was real work! The radio was packed in a water-resistant rubberized canvas pouch and it would float. Included in the pouch were two antennas, a grounding mechanism, a spool of wire, and a box kite. One of the antenna was a 12-ft. whip, but the neatest idea was the long wire antenna. The box kite was made of aluminum rods and canvas and was slightly larger than the wood and paper kites that are sold today. The idea was to use the wire included as the kite "string" and as the long wire antenna. Remember, this radio operated at 500 kHz and at 8 MHz. The grounding device was a weight on the end of a length of copper braid. It was supposed to be pitched over the side when you wanted to transmit. The instructions were printed on a placard attached to the radio. I don't remember what their recommendations were about flying the kite during electrical storms. We removed these radios from life rafts and tested them once a year inside a screen room.

Several years after being in the service I bought one of the kites at a surplus store. I still have it as it is a terrific flyer (when the wind is above 10 mph). Thanks for reminding me of the pleasures of checking "Gibson Girl" radios.

DAVID E. ZIMMERMAN
GRASS VALLEY GROUP
GRASS VALLEY, CALIF.

...OR THE COFFEE GRINDER

The radio mentioned may have been one of the "Gibson Girl" or "Coffee Grinder" series. It gained the first name by its pinched-in center to fit between the legs of a person seated in a life raft and the

second due to the crank operating handle on the top. There were no batteries; the crank drove a generator for filament and high-voltage supplies and also drove the encoder for transmitting "SOS." The RF output was a mighty 1 W and the output switched between 500 kHz and 8.364 MHz every few turns of the handle. I first came across one when I was 19 years old and fresh out of high school, where I had been on the wrestling team. Nonetheless, I found it very tiring to turn the handle while testing one on a repair bench. I wonder how a person in a tiny lifeboat could have operated one in a weakened condition.

The extreme weight was due to the dc generator—a very robust cast aluminum case—the ground line and weight which were to be dropped over the side, an antenna line, and a kite and balloon for raising the antenna. There was a cylinder of helium for inflating the balloon.

I doubt that the unit could have been effective since the antenna tuning could only have been an approximation, but maybe the kite provided some entertainment. The requirement for ships to monitor these emergency frequencies the first 10 minutes of every hour has recently been rescinded.

Now with satellites, emergency contact is reasonably assured. Beam me up, Scotty!

GIL PILZ
FLO-TECH INC.
MUNDELEIN, ILL.

...AND IT'S STILL AVAILABLE

We also heard from Eric Kinast, Sonntek Inc., Woodcliff Lake, N.J., who, like the others, pointed out the hand-cranked generator. Kinast included a clipping from a surplus dealer's current catalog, which offered the MacKay Model 401A for $149.50. However, the item included a cautionary note: "These units do not meet current standards for emergency rescue equipment. Sold AS IS. Should be used for parts or display only."—Ed.

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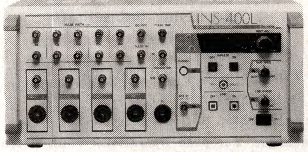

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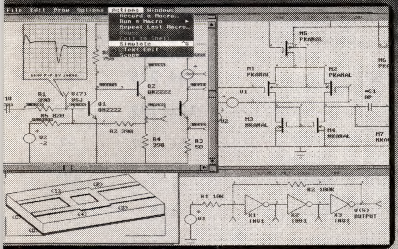

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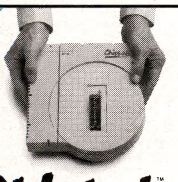

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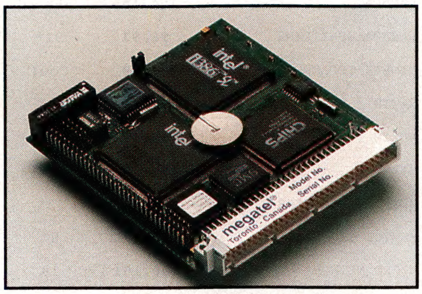

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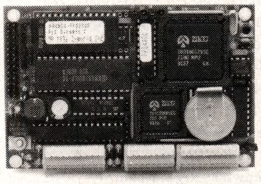

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